



## ASI-T-570EA14QN/D

Item	Contents	Unit
LCD Type	a-Si TFT Active Matrix	
Display Mode	Normally White / Transmmissive	
Viewing Direction	6:00	
Interface	8 bit parallel / serial	
Number of Dots/ characters	320 X 240 Dots	
Dot Pitch (W×H)	0.36X0.36	mm
Active Area	115.2×86.4	mm
Outline Dimension (W x H x D)	159.50×108.40×6.35	mm
Driver IC	ST7511	
Display Format	Mono Stripe Type	
Backlight Type	LED	
Backlight Color	White	
Operating Temperature	-20°C~+70°C	
Storage Temperature	-30°C~+80°C	



Record of Revision

Date	Revision No.	Summary
2015-09-12	1.0	Rev 1.0 was issued



## ASI-T-570EA14QN/D

### 1. Scope

This data sheet is to introduce the specification of ASI-T-570EA14QN/D active matrix TFT module. It is composed of a Mono TFT-LCD panel, driver ICs, FPC, and a backlight unit. The 8.0" display area contains 320(RGB) x 240.

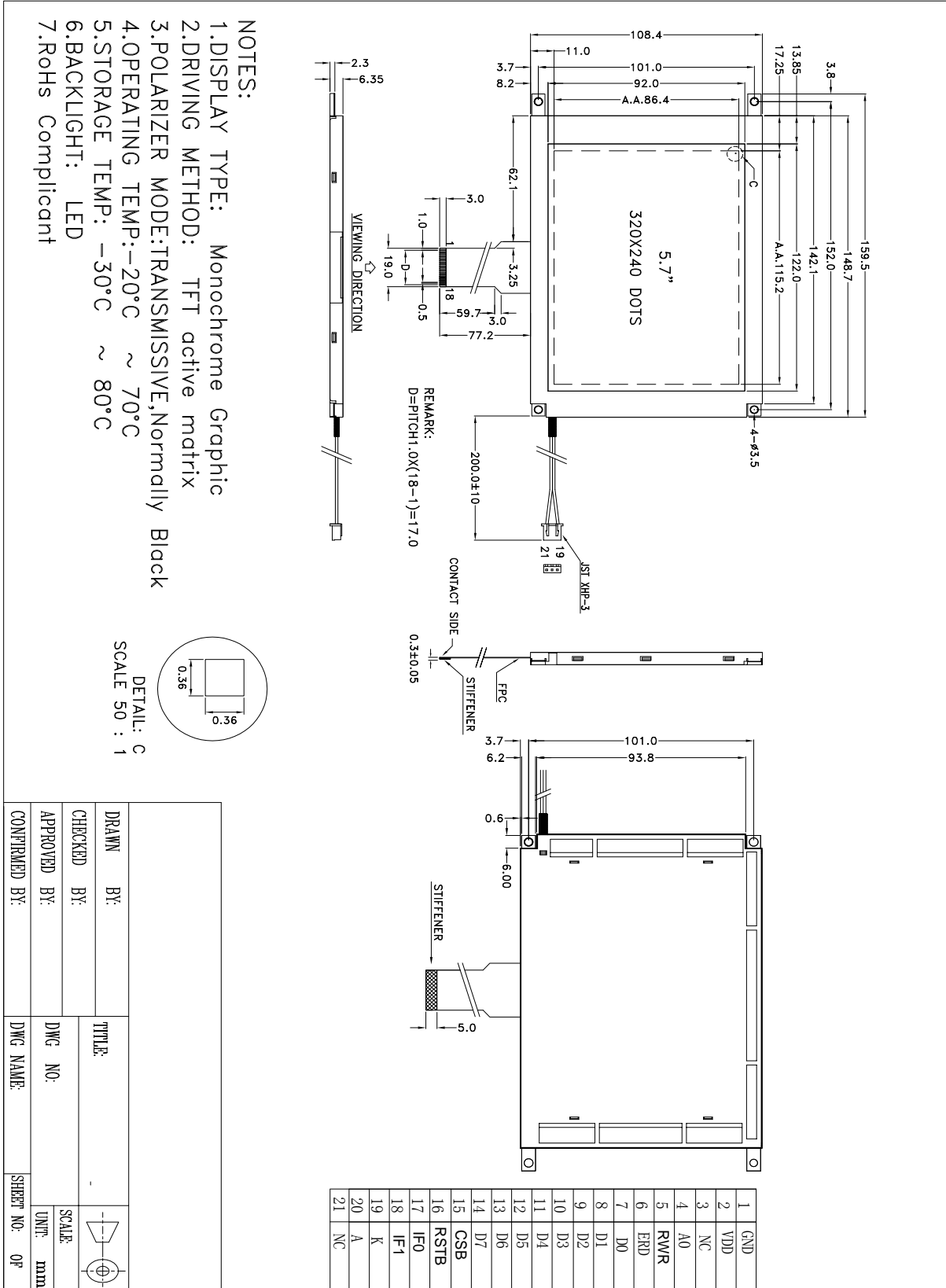
### 2. Application

Digital equipments which need display, instrumentation, remote control, electronic product.

### 3. General Information

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4. Outline Drawing



5. Interface signals

Pin No.	Symbol	Description
1	GND	Ground
2	VDD	Supply logic power
3	NC	No connection
4	A0	Register select
5	RWR	Read / Write operation control
6	ERD	Read / Write operation control
7	D0	Data bit0
8	D1	Data bit1
9	D2	Data bit2
10	D3	Data bit3
11	D4	Data bit4
12	D5	Data bit5
13	D6	Data bit6
14	D7	Data bit7
15	CSB	Chip select
16	RSTB	Reset
17	IF0	Microprocessor type select
18	IF1	Interface select
19	K	Supply Voltage for Backlight (-)
20	NC	No connection
21	A	Supply Voltage for Backlight (+)

## 6. Absolute maximum Ratings

### 6.1. Electrical Absolute max. ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Supply Voltage	VDD	-0.3	6.0	V	
Input Voltage	VT	-0.3	VDD +0.3	V	

### 6.2. Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-20	70	°C	
Storage Temperature	TSTG	-30	80	°C	

## 7. Electrical Specifications

### 7.1 Electrical characteristics

GND=0V, Ta=25°C

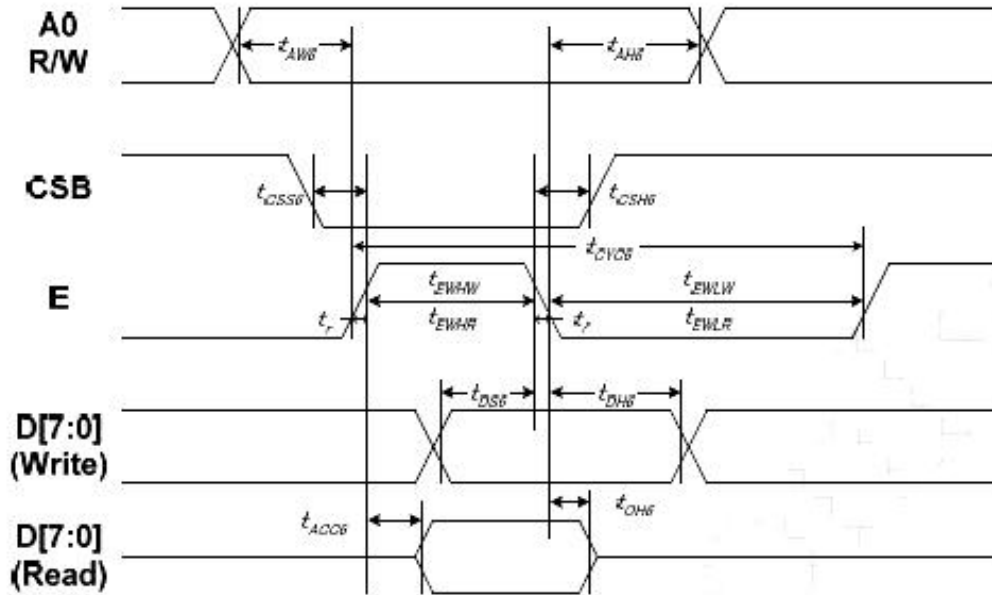
Item	Symbol	MIN	TYP	MAX	Unit	Remark
Logic Supply Voltage	VDD	3.05	3.3	3.55	V	
Input Signal Voltage	High VIH	0.8VDD	--	VDD	V	
	Low VIL	0	--	0.2VDD	V	

### 7.2 Backlight

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward current	If	--	120	--	mA	
Forward voltage	VF	8.4	9.0	9.6	V	

## 8. Command/AC Timing

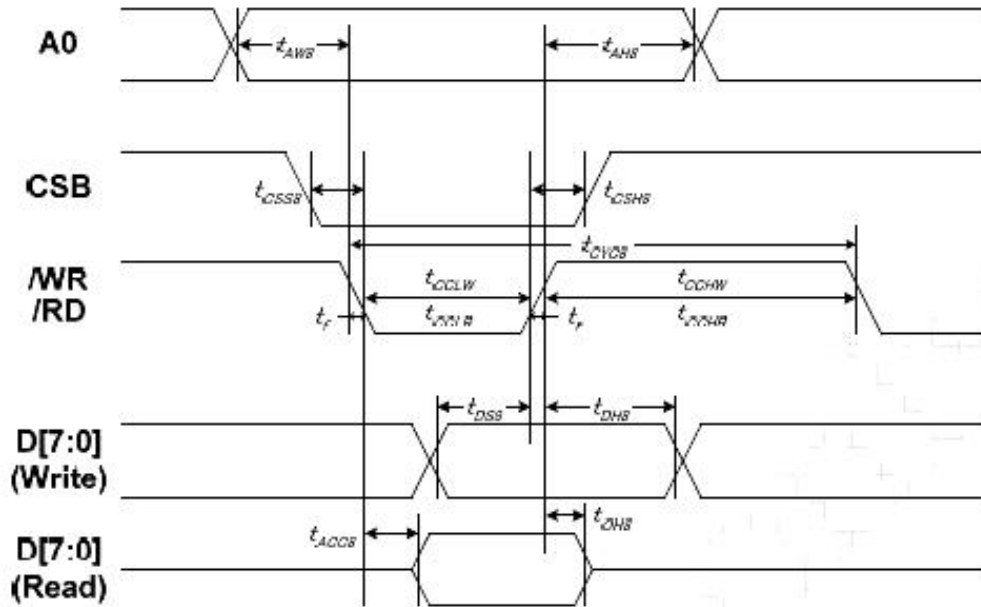
### 8.1 6800 Interface timing



AGND = PGND = DGND = 0V, VDDA = VDDP = VDDI = 3.0 ~ 5.0V, T<sub>a</sub> = 25°C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	t <sub>AW6</sub>		10	—	ns
Address hold time		t <sub>AH6</sub>		0	—	
System cycle time	E	t <sub>CYC6</sub>		1100	—	
Enable L pulse width (WRITE)		t <sub>EHLW</sub>		500	—	
Enable H pulse width (WRITE)		t <sub>EHWL</sub>		500	—	
Enable L pulse width (READ)		t <sub>EHLR</sub>		500	—	
Enable H pulse width (READ)	t <sub>EHWR</sub>		500	—		
CSB setup time	CSB	t <sub>CSS6</sub>		100	—	
CSB hold time		t <sub>CSH6</sub>		130	—	
Write data setup time	D[7:0]	t <sub>DS6</sub>		200	—	
Write data hold time		t <sub>DH6</sub>		250	—	
Read data access time		t <sub>ACC6</sub>	CL = 100 pF	—	950	
Read data output disable time		t <sub>OH6</sub>	CL = 100 pF	5	200	

8.2 8080 Interface timing

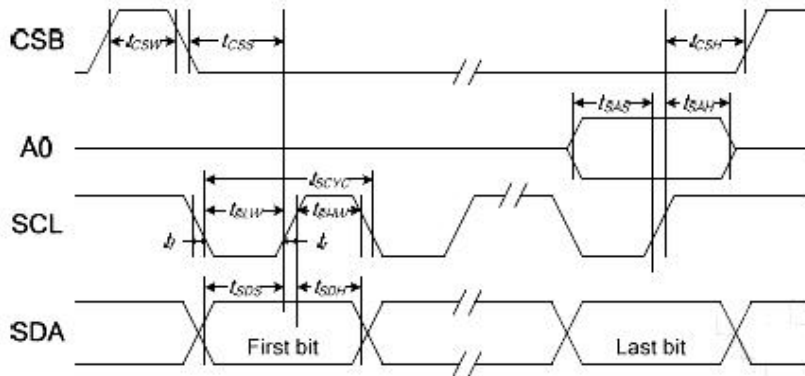


AGND = PGND = DGND = 0V, VDDA = VDDP = VDDI = 3.0 ~ 5.0V, Ta = 25°C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAWS		10	—	ns
Address hold time		tAHS		0	—	
System cycle time	/WR	tCYC8		1100	—	
/WR L pulse width (WRITE)		tCCLW		500	—	
/WR H pulse width (WRITE)		tCCHW		500	—	
/RD L pulse width (READ)		/RD	tCCLR		950	
/RD H pulse width (READ)	tCCHR			500	—	
CSB setup time	CSB	tCSS8		100	—	
CSB hold time		tCSH8		100	—	
WRITE Data setup time	D[7:0]	tDS8		200	—	
WRITE Data hold time		tDH8		50	—	
READ access time		tACC8	CL = 100 pF	—	950	
READ Output disable time		tOH8	CL = 100 pF	5	200	

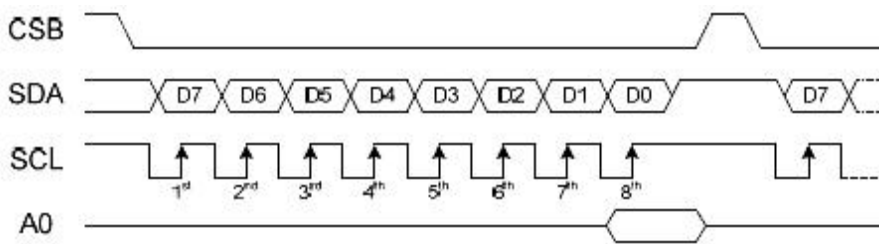


8.3 4-Line serial interface timing

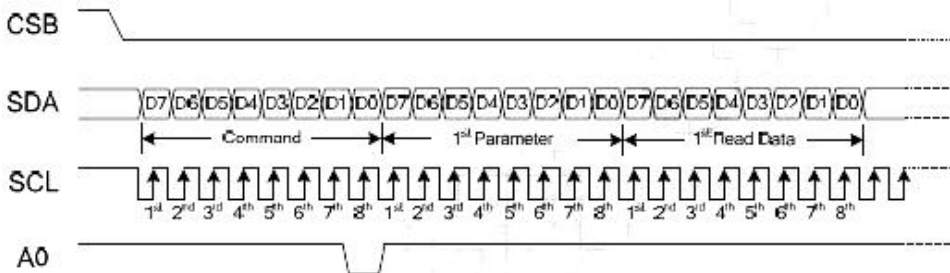


AGND = PGND = DGND = 0V, VDDA = VDDP = VDDI = 3.0 ~ 5.0V, Ta = 25°C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period		tSCYC		300	—	ns
SCL "H" pulse width	SCL	tSHW		150	—	
SCL "L" pulse width	SCL	tSLW		150	—	
Address setup time	A0	tSAS		150	—	
Address hold time	A0	tSAH		150	—	
Data setup time	SDA	tSDS		120	—	
Data hold time	SDA	tSDH		120	—	
CSB-SCL time		tCSS		150	—	
CSB-SCL time	CSB	tCSH		150	—	
CSB "H" pulse width		tCSW		30	—	

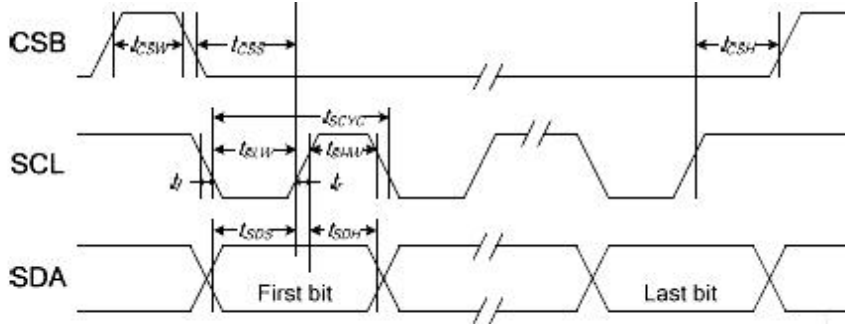


Write-Operation of 4-Line Serial Interface



Read-Operation of 4-Line Serial Interface

8.4 3-Line serial interface timing



AGND = PGND = DGND = 0V, VDDA = VDDP = VDDI = 3.0 ~ 5.0V, Ta = 25°C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial Clock Period	SCL	tSCYC		300	—	ns
SCL "H" pulse width		tSHW		150	—	
SCL "L" pulse width		tSLW		150	—	
Data setup time	SDA	tSDS		120	—	
Data hold time		tSDH		120	—	
CSB-SCL time	CSB	tCSS		150	—	
CSB-SCL time		tCSH		150	—	
CSB "H" pulse width		tCSW		30	—	

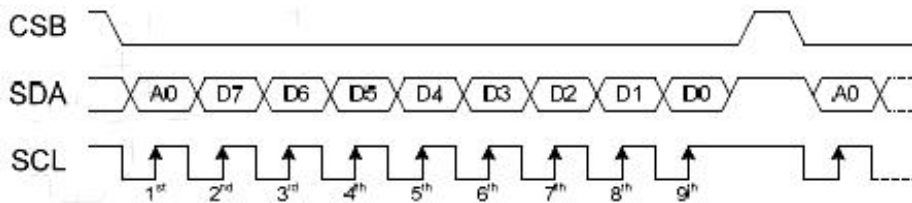
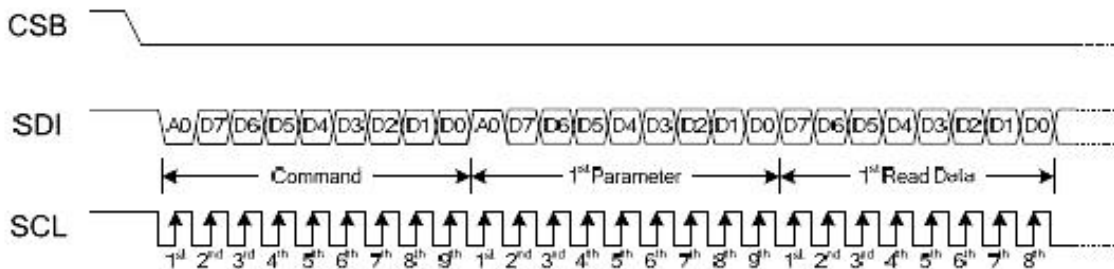
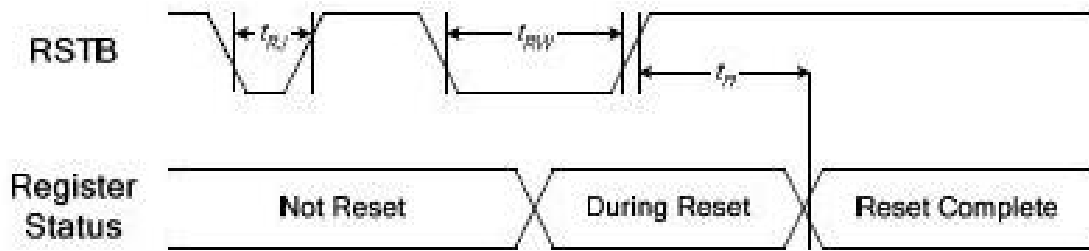


Fig 3 Write-Operation of 3-Line Serial Interface



Read-Operation of 3-Line Serial Interface

8.5 Reset timing



AGND = PGND = DGND = 0V, VDDA = VDDP = VDDI = 3.0 ~ 5.0V, Ta = 25°C

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Reset time	RSTB	tR		—	5 <sup>-1</sup>	us
Reset "L" pulse width		tRW		15	—	
Reset rejection		tRJ		—	5	
Reset rejection (for noise spike)		tRJS		—	10	ns

THE RESET OF CIRCUIT

Setting RSTB pin to "L" (hardware reset) can initialize internal function. Generally, VDDI is not stable at the time that the system power is just turned ON. The hardware reset or software reset is required to initialize internal registers after VDDI is stable. Initialization by RSTB pin or command SWRESET is essential before operating

8.6 INSTRUCTIONS TABLE

Instruction	Add. (hex)	A0	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	Function
NOP	00	0	1	↑	0	0	0	0	0	0	0	0		Non-Operation
		1	1	↑	1	0	1	0	0	1	0	1		
SLPOUT	12	0	1	↑	0	0	0	1	0	0	1	0		Sleep Out
		1	1	↑	1	0	1	0	0	1	0	1		
SLPIN	13	0	1	↑	0	0	0	1	0	0	1	1		Sleep In
		1	1	↑	1	0	1	0	0	1	0	1		
DISOFF	14	0	1	↑	0	0	0	1	0	1	0	0		Display Off
		1	1	↑	1	0	1	0	0	1	0	1		
DISON	15	0	1	↑	0	0	0	1	0	1	0	1		Display On
		1	1	↑	1	0	1	0	0	1	0	1		
DINVOUT	1A	0	1	↑	0	0	0	1	1	0	1	0		Display Invert Out
		1	1	↑	1	0	1	0	0	1	0	1		
DINVIN	1B	0	1	↑	0	0	0	1	1	0	1	1		Display Invert In
		1	1	↑	1	0	1	0	0	1	0	1		
BLOUT	1C	0	1	↑	0	0	0	1	1	1	0	0		Blinking Out
		1	1	↑	1	0	1	0	0	1	0	1		
BLIN	1D	0	1	↑	0	0	0	1	1	1	0	1		Blinking In
		1	1	↑	1	0	1	0	0	1	0	1		
STFRAME	21	0	1	↑	0	0	1	0	0	0	0	1	00	Start Frame Address
		1	1	↑	0	0	0	0	0	0	SFmA1	SFmA0		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
BPPSEL	22	0	1	↑	0	0	1	0	0	0	1	0	02	BPP Select
		1	1	↑	0	0	0	0	0	0	BppSel1	BppSel0		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
MADCTL	24	0	1	↑	0	0	1	0	0	1	0	0	00	Memory Address Control
		1	1	↑	0	0	0	0	0	MV	MY	MX		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
PASET	25	0	1	↑	0	0	1	0	0	1	0	1	00	Page Address Set
		1	1	↑	PSA7	PSA6	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0		
		1	1	↑	PEA7	PEA6	PEA5	PEA4	PEA3	PEA2	PEA1	PEA0		
		1	1	↑	0	0	0	0	0	0	FmA1	FmA0		
CASET	26	0	1	↑	0	0	1	0	0	1	1	0		Column



# ASI-T-570EA14QN/D

		1	1	↑	0	0	0	0	0	0	CSA9	CSA8	00	Address Set				
		1	1	↑	CSA7	CSA6	CSA5	CSA4	CSA3	CSA2	CSA1	CSA0	00		Address Set			
		1	1	↑	0	0	0	0	0	0	CEA9	CEA8	02			Address Set		
		1	1	↑	CEA7	CEA6	CEA5	CEA4	CEA3	CEA2	CEA1	CEA0	7F				Address Set	
BLKFIL	29	0	1	↑	0	0	1	0	1	0	0	1		Block Fill				
		1	1	↑	0	0	0	0	BFDat3	BFDat2	BFDat1	BFDat0	00		Block Fill			
		1	1	↑	1	0	1	0	0	1	0	1				Block Fill		
		1	1	↑	1	0	1	0	0	1	0	1					Block Fill	
BLGET	2B	0	1	↑	0	0	1	0	1	0	1	1		Blinking Set				
		1	1	↑	BlinkCyc7	BlinkCyc6	BlinkCyc5	BlinkCyc4	BlinkCyc3	BlinkCyc2	BlinkCyc1	BlinkCyc0	1D		Blinking Set			
		1	1	↑	0	0	0	0	B1stF1	B1stF0	B2ndF1	B2ndF0	01			Blinking Set		
		1	1	↑	1	0	1	0	0	1	0	1					Blinking Set	
WRRAM	2C	0	1	↑	0	0	1	0	1	1	0	0		Write RAM				
		1	1	↑	1	0	1	0	0	1	0	1			Write RAM			
		1	1	↑	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0				Write RAM		
RDRAM	2D	0	1	↑	0	0	1	0	1	1	0	1		Read RAM				
		1	1	↑	1	0	1	0	0	1	0	1			Read RAM			
		1	↑	1	X	X	X	X	X	X	X	X	X				Read RAM	
		1	↑	1	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0				Read RAM		
DISAR	31	0	1	↑	0	0	1	1	0	0	0	1		Display Area				
		1	1	↑	0	0	0	0	0	0	0	DisLin8	01		Display Area			
		1	1	↑	DisLin7	DisLin6	DisLin5	DisLin4	DisLin3	DisLin2	DisLin1	DisLin0	3F				Display Area	
		1	1	↑	0	0	0	0	0	0	0	DisCol9	DisCol8			02		Display Area
		1	1	↑	DisCol7	DisCol6	DisCol5	DisCol4	DisCol3	DisCol2	DisCol1	DisCol0	7F			Display Area		
DISSET1	32	0	1	↑	0	0	1	1	0	0	1	0		Display Set1				
		1	1	↑	HClkNo7	HClkNo6	HClkNo5	HClkNo4	HClkNo3	HClkNo2	HClkNo1	HClkNo0	32		Display Set1			
		1	1	↑	BPN07	BPN06	BPN05	BPN04	BPN03	BPN02	BPN01	BPN00	02				Display Set1	
		1	1	↑	NorBlk	OSCO	0	0	FPNo11	FPNo10	FPNo9	FPNo8	00					Display Set1
		1	1	↑	FPNo7	FPNo6	FPNo5	FPNo4	FPNo3	FPNo2	FPNo1	FPNo0	01			Display Set1		
DISSET2	33	0	1	↑	0	0	1	1	0	0	1	1		Display Set2				
		1	1	↑	SOnt7	SOnt6	SOnt5	SOnt4	SOnt3	SOnt2	SOnt1	SOnt0	0A		Display Set2			
		1	1	↑	SOft7	SOft6	SOft5	SOft4	SOft3	SOft2	SOft1	SOft0	28				Display Set2	
		1	1	↑	GOnt7	GOnt6	GOnt5	GOnt4	GOnt3	GOnt2	GOnt1	GOnt0	0C					Display Set2
		1	1	↑	GOft7	GOft6	GOft5	GOft4	GOft3	GOft2	GOft1	GOft0	26			Display Set2		
PTLSET1	34	0	1	↑	0	0	1	1	0	1	0	0		Partial Set 1				
		1	1	↑	0	0	0	0	0	0	0	Part1SL8	00		Partial Set 1			
		1	1	↑	Part1SL7	Part1SL6	Part1SL5	Part1SL4	Part1SL3	Part1SL2	Part1SL1	Part1SL0	00				Partial Set 1	
		1	1	↑	0	0	0	0	0	0	0	Part1EL8	00					Partial Set 1
		1	1	↑	Part1EL7	Part1EL6	Part1EL5	Part1EL4	Part1EL3	Part1EL2	Part1EL1	Part1EL0	00			Partial Set 1		
PTLSET2	35	0	1	↑	0	0	1	1	0	1	0	1		Partial Set 2				
		1	1	↑	0	0	0	0	0	0	0	Part2SL8	00		Partial Set 2			
		1	1	↑	Part2SL7	Part2SL6	Part2SL5	Part2SL4	Part2SL3	Part2SL2	Part2SL1	Part2SL0	00				Partial Set 2	
		1	1	↑	0	0	0	0	0	0	0	Part2EL8	00					Partial Set 2
		1	1	↑	0	0	0	0	0	0	0	Part2EL8	00			Partial Set 2		

		1	1	↑	Part2EL7	Part2EL6	Part2EL5	Part2EL4	Part2EL3	Part2EL2	Part2EL1	Part2EL0	00		
PTLSET3	36	0	1	↑	0	0	1	1	0	1	1	0		Partial Set 3	
		1	1	↑	0	NDIsRefR6	NDIsRefR5	NDIsRefR4	NDIsRefR3	NDIsRefR2	NDIsRefR1	NDIsRefR0	00		
		1	1	↑	0	0	0	0	0	0	RTBFreq2	RTBFreq1	RTBFreq0		00
		1	1	↑	0	0	0	0	0	0	0	NDIsDM1	NDIsDM0		00
		1	1	↑	1	0	1	0	0	1	0	0	1		
VCM DAT	54	0	1	↑	0	1	0	1	0	1	0	0		VCOM Offset Data	
		1	1	↑	0	0	0	0	VcomS3	VcomS2	VcomS1	VcomS0	00		
		1	1	↑	0	0	VcomD15	VcomD14	VcomD13	VcomD12	VcomD11	VcomD10	00		
		1	1	↑	0	0	VcomD25	VcomD24	VcomD23	VcomD22	VcomD21	VcomD20	00		
		1	1	↑	1	0	1	0	0	1	0	1			
UIDSET	55	0	1	↑	0	1	0	1	0	1	0	1		User ID	
		1	1	↑	UID117	UID116	UID115	UID114	UID113	UID112	UID111	UID110	00		
		1	1	↑	UID127	UID126	UID125	UID124	UID123	UID122	UID121	UID120	00		
		1	1	↑	UID217	UID216	UID215	UID214	UID213	UID212	UID211	UID210	00		
		1	1	↑	UID227	UID226	UID225	UID224	UID223	UID222	UID221	UID220	00		
MTPMOD	5A	0	1	↑	0	1	0	1	1	0	1	0		Multi Time PROM Mode	
		1	1	↑	MTPMOD7	MTPMOD6	MTPMOD5	MTPMOD4	MTPMOD3	MTPMOD2	MTPMOD1	MTPMOD0	00		
		1	1	↑	1	0	1	0	0	1	0	1			
		1	1	↑	1	0	1	0	0	1	0	1			
		1	1	↑	1	0	1	0	0	1	0	1			
MTPOP	5B	0	1	↑	0	1	0	1	1	0	1	1		Multi Time PROM Operation	
		1	1	↑	0	0	0	0	0	MTP_Sel	0	Prog_Mod	00		
		1	1	↑	1	0	1	0	0	1	0	1			
		1	1	↑	1	0	1	0	0	1	0	1			
		1	1	↑	1	0	1	0	0	1	0	1			
PWRCTL	61	0	1	↑	0	1	1	0	0	0	0	1		Power Control	
		1	1	↑	BST3SR1	BST3SR0	0	0	BST4ON	BST3ON	BST2ON	BST1ON	40		
		1	1	↑	FOFNo3	FOFNo2	FOFNo1	FOFNo0	0	SAMPSet2	SAMPSet1	SAMPSet0	01		
		1	1	↑	0	0	0	0	0	0	1	0	02		
		1	1	↑	1	0	1	0	0	1	0	1			
EVSET1	62	0	1	↑	0	1	1	0	0	0	1	0		Electronic Volumn Set 1	
		1	1	↑	0	VCOM6	VCOM5	VCOM4	VCOM3	VCOM2	VCOM1	VCOM0	0A		
		1	1	↑	0	0	VGHREG5	VGHREG4	VGHREG3	VGHREG2	VGHREG1	VGHREG0	06		
		1	1	↑	0	0	0	VGLREG4	VGLREG3	VGLREG2	VGLREG1	VGLREG0	0F		
		1	1	↑	1	0	1	0	0	1	0	1			
EVSET2	63	0	1	↑	0	1	1	0	0	0	1	1		Electronic Volumn Set 2	
		1	1	↑	0	0	0	GVDD4	GVDD3	GVDD2	GVDD1	GVDD0	0F		
		1	1	↑	0	0	0	GVCL4	GVCL3	GVCL2	GVCL1	GVCL0	0F		
		1	1	↑	1	0	1	0	0	1	0	1			
		1	1	↑	1	0	1	0	0	1	0	1			
BCLKSET	64	0	1	↑	0	1	1	0	0	1	0	0		Booster Clock Setting	
		1	1	↑	0	AVdClk2	AVdClk1	AVdClk0	0	AVdClk2	AVdClk2	AVdClk2	44		
		1	1	↑	0	VgIClk2	VgIClk1	VgIClk0	0	VghClk2	VghClk1	VghClk0	44		
		1	1	↑	0	AVdClk_nd1	AVdClk_nd1	AVdClk_nd2	0	AVdClk_nd2	AVdClk_nd1	AVdClk_nd0	44		



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		1	1	↑	0	VgClk_Lnd2	VgClk_Lnd1	VgClk_Lnd0	0	VghClk_Lnd2	VghClk_Lnd1	VghClk_Lnd0	44	
GATESET	66	0	1	↑	0	1	1	0	0	1	1	0		Gate Set
		1	1	↑	VGPP	0	0	ScanDir	0	0	ScanMod1	ScanMod0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
PWMCTRL	60	0	1	↑	0	1	1	0	1	1	0	0		PWM Control
		1	1	↑	0	0	0	0	0	LOnTyp	0	LEDMD	00	
		1	1	↑	SLEDOn7	SLEDOn6	SLEDOn5	SLEDOn4	SLEDOn3	SLEDOn2	SLEDOn1	SLEDOn0		
		1	1	↑	ASLEDOn7	ASLEDOn6	ASLEDOn5	ASLEDOn4	ASLEDOn3	ASLEDOn2	ASLEDOn1	ASLEDOn0		
RDSTAT	72	1	1	↑	ASLEDOF7	ASLEDOF6	ASLEDOF5	ASLEDOF4	ASLEDOF3	ASLEDOF2	ASLEDOF1	ASLEDOF0		
		0	1	↑	0	1	1	1	0	0	1	0		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	R17	R16	R15	0	R13	R12	R11	R10		
		1	↑	1	0	R26	R25	R24	R23	R22	R21	R20		
		1	↑	1	R37	R36	R35	R34	R33	R32	R31	R30		
		1	↑	1	R47	R46	R45	R44	R43	R42	R41	R40		
RDREV	73	1	↑	1	0	0	0	0	R52	R51	R50			
		1	↑	1	0	R66	R65	R64	0	R62	R61	R60		
		0	1	↑	0	1	1	1	0	0	1	1		
RDUID	75	1	1	↑	1	0	1	0	0	1	0	1		Read User ID
		1	↑	1	R17	R16	R15	R14	R13	R12	R11	R10		
		1	↑	1	R27	R26	R25	R24	R23	R22	R21	R20		
		1	↑	1	R37	R36	R35	R34	R33	R32	R31	R30		
		1	↑	1	R47	R46	R45	R44	R43	R42	R41	R40		
		1	↑	1	R57	R56	R55	R54	R53	R52	R51	R50		
		1	↑	1	R67	R66	R65	R64	R63	R62	R61	R60		
		1	↑	1	R77	R76	R75	R74	R73	R72	R71	R70		
		1	↑	1	R87	R86	R85	R84	R83	R82	R81	R80		
		1	↑	1	R97	R96	R95	R94	R93	R92	R91	R90		
		1	↑	1	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0		
		1	↑	1	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0		
		1	↑	1	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0		
RDVCMDAT	79	0	1	↑	0	1	1	1	1	0	0	1		Read VCOM Data
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	x	x	R15	R14	R13	R12	R11	R10		
		1	↑	1	x	x	R25	R24	R23	R22	R21	R20		
		1	↑	1	x	x	R35	R34	R33	R32	R31	R30		
		1	↑	1	x	x	R45	R44	R43	R42	R41	R40		
		1	↑	1	x	x	R55	R54	R53	R52	R51	R50		
		1	↑	1	x	x	R65	R64	R63	R62	R61	R60		
1	↑	1	x	x	R75	R74	R73	R72	R71	R70				



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		1	↑	↑	0	0	0	0	R83	R82	R81	R80		
GAMSET4 P1	91	0	1	↑	1	0	0	1	0	0	0	1		
		1	1	↑	0	0	G4BPV05	G4BPV04	G4BPV03	G4BPV02	G4BPV01	G4BPV00	00	Gamma Set
		1	1	↑	0	0	G4BPV15	G4BPV14	G4BPV13	G4BPV12	G4BPV11	G4BPV10	04	4bpp
		1	1	↑	0	0	G4BPV25	G4BPV24	G4BPV23	G4BPV22	G4BPV21	G4BPV20	08	Positive 1
		1	1	↑	0	0	G4BPV35	G4BPV34	G4BPV33	G4BPV32	G4BPV31	G4BPV30	DC	
GAMSET4 P2	92	0	1	↑	1	0	0	1	0	0	1	0		
		1	1	↑	0	0	G4BPV45	G4BPV44	G4BPV43	G4BPV42	G4BPV41	G4BPV40	10	Gamma Set
		1	1	↑	0	0	G4BPV55	G4BPV54	G4BPV53	G4BPV52	G4BPV51	G4BPV50	14	4bpp
		1	1	↑	0	0	G4BPV65	G4BPV64	G4BPV63	G4BPV62	G4BPV61	G4BPV60	18	Positive 2
		1	1	↑	0	0	G4BPV75	G4BPV74	G4BPV73	G4BPV72	G4BPV71	G4BPV70	1C	
GAMSET4 P3	93	0	1	↑	1	0	0	1	0	0	1	1		
		1	1	↑	0	0	G4BPV85	G4BPV84	G4BPV83	G4BPV82	G4BPV81	G4BPV80	23	Gamma Set
		1	1	↑	0	0	G4BPV95	G4BPV94	G4BPV93	G4BPV92	G4BPV91	G4BPV90	27	4bpp
		1	1	↑	0	0	G4BPVA5	G4BPVA4	G4BPVA3	G4BPVA2	G4BPVA1	G4BPVA0	2B	Positive 3
		1	1	↑	0	0	G4BPVB5	G4BPVB4	G4BPVB3	G4BPVB2	G4BPVB1	G4BPVB0	2F	
GAMSET4 P4	94	0	1	↑	1	0	0	1	0	1	0	0		
		1	1	↑	0	0	G4BPVC5	G4BPVC4	G4BPVC3	G4BPVC2	G4BPVC1	G4BPVC0	33	Gamma Set
		1	1	↑	0	0	G4BPVD5	G4BPVD4	G4BPVD3	G4BPVD2	G4BPVD1	G4BPVD0	37	4bpp
		1	1	↑	0	0	G4BPVE5	G4BPVE4	G4BPVE3	G4BPVE2	G4BPVE1	G4BPVE0	3B	Positive 4
		1	1	↑	0	0	G4BPVF5	G4BPVF4	G4BPVF3	G4BPVF2	G4BPVF1	G4BPVF0	3F	
GAMSET2 P	95	0	1	↑	1	0	0	1	0	1	0	1		
		1	1	↑	0	0	G2BPV05	G2BPV04	G2BPV03	G2BPV02	G2BPV01	G2BPV00	00	Gamma Set
		1	1	↑	0	0	G2BPV15	G2BPV14	G2BPV13	G2BPV12	G2BPV11	G2BPV10	15	2bpp
		1	1	↑	0	0	G2BPV25	G2BPV24	G2BPV23	G2BPV22	G2BPV21	G2BPV20	2A	Positive
		1	1	↑	0	0	G2BPV35	G2BPV34	G2BPV33	G2BPV32	G2BPV31	G2BPV30	3F	
GAMSET1	96	0	1	↑	1	0	0	1	0	1	1	0		
		1	1	↑	0	0	G1BPV05	G1BPV04	G1BPV03	G1BPV02	G1BPV01	G1BPV00	00	Gamma Set
		1	1	↑	0	0	G1BPV15	G1BPV14	G1BPV13	G1BPV12	G1BPV11	G1BPV10	3F	1bpp
		1	1	↑	0	0	G1BNV05	G1BNV04	G1BNV03	G1BNV02	G1BNV01	G1BNV00	00	
		1	1	↑	0	0	G1BNV15	G1BNV14	G1BNV13	G1BNV12	G1BNV11	G1BNV10	3F	
GAMSET4 N1	99	0	1	↑	1	0	0	1	1	0	0	1		
		1	1	↑	0	0	G4BNV05	G4BNV04	G4BNV03	G4BNV02	G4BNV01	G4BNV00	00	Gamma Set
		1	1	↑	0	0	G4BNV15	G4BNV14	G4BNV13	G4BNV12	G4BNV11	G4BNV10	04	4bpp
		1	1	↑	0	0	G4BNV25	G4BNV24	G4BNV23	G4BNV22	G4BNV21	G4BNV20	08	Negative 1
		1	1	↑	0	0	G4BNV35	G4BNV34	G4BNV33	G4BNV32	G4BNV31	G4BNV30	DC	
GAMSET4 N2	9A	0	1	↑	1	0	0	1	1	0	1	0		
		1	1	↑	0	0	G4BNV45	G4BNV44	G4BNV43	G4BNV42	G4BNV41	G4BNV40	10	Gamma Set
		1	1	↑	0	0	G4BNV55	G4BNV54	G4BNV53	G4BNV52	G4BNV51	G4BNV50	14	4bpp
		1	1	↑	0	0	G4BNV65	G4BNV64	G4BNV63	G4BNV62	G4BNV61	G4BNV60	18	Negative 2
		1	1	↑	0	0	G4BNV75	G4BNV74	G4BNV73	G4BNV72	G4BNV71	G4BNV70	1C	
GAMSET4 N3	9B	0	1	↑	1	0	0	1	1	0	1	1		
		1	1	↑	0	0	G4BNV85	G4BNV84	G4BNV83	G4BNV82	G4BNV81	G4BNV80	23	Gamma Set
		1	1	↑	0	0	G4BNV95	G4BNV94	G4BNV93	G4BNV92	G4BNV91	G4BNV90	27	4bpp
		1	1	↑	0	0	G4BNVA5	G4BNVA4	G4BNVA3	G4BNVA2	G4BNVA1	G4BNVA0	2B	Negative 3





		1	1	↑	0	0	G4BNVB5	G4BNVB4	G4BNVB3	G4BNVB2	G4BNVB1	G4BNVB0	2F	
GAMSET4 N4	9C	0	1	↑	1	0	0	1	1	1	0	0		Gamma Set 4bpp Negative 4
		1	1	↑	0	0	G4BNVC5	G4BNVC4	G4BNVC3	G4BNVC2	G4BNVC1	G4BNVC0	33	
		1	1	↑	0	0	G4BNVD5	G4BNVD4	G4BNVD3	G4BNVD2	G4BNVD1	G4BNVD0	37	
		1	1	↑	0	0	G4BNVE5	G4BNVE4	G4BNVE3	G4BNVE2	G4BNVE1	G4BNVE0	3B	
		1	1	↑	0	0	G4BNVF5	G4BNVF4	G4BNVF3	G4BNVF2	G4BNVF1	G4BNVF0	3F	
GAMSET2 N	9D	0	1	↑	1	0	0	1	1	1	0	1		Gamma Set 2bpp Negative
		1	1	↑	0	0	G2BNV05	G2BNV04	G2BNV03	G2BNV02	G2BNV01	G2BNV00	00	
		1	1	↑	0	0	G2BNV15	G2BNV14	G2BNV13	G2BNV12	G2BNV11	G2BNV10	15	
		1	1	↑	0	0	G2BNV25	G2BNV24	G2BNV23	G2BNV22	G2BNV21	G2BNV20	2A	
		1	1	↑	0	0	G2BNV35	G2BNV34	G2BNV33	G2BNV32	G2BNV31	G2BNV30	3F	
RMWIN	A1	0	1	↑	1	0	1	0	0	0	0	1		Read Modify Write In
		1	1	↑	1	0	1	0	0	1	0	1		
MTPRDEN	A2	0	1	↑	1	0	1	0	0	0	1	0		MTP Read Enable
		1	1	↑	1	0	1	0	0	1	0	1		
MTPWREN	A3	0	1	↑	1	0	1	0	0	0	1	1		MTP Write Enable
		1	1	↑	1	0	1	0	0	1	0	1		
PTLOUT	A9	0	1	↑	1	0	1	0	1	0	0	1		Partial Out
		1	1	↑	1	0	1	0	0	1	0	1		
PTLIN	AA	0	1	↑	1	0	1	0	1	0	1	0		Partial In
		1	1	↑	1	0	1	0	0	1	0	1		
RMWOUT	AC	0	1	↑	1	0	1	0	1	1	0	0		Read Modify Write Out
		1	1	↑	1	0	1	0	0	1	0	1		
SWRESET	AE	0	1	↑	1	0	1	0	1	1	1	0		Software Reset
		1	1	↑	1	0	1	0	0	1	0	1		

**RECOMMENDED INITIAL SETTINGS**

- Software Reset: AEH,A5H
- Power Control: 61H,0FH,04H,02H,A5H
- Electronic Volume Set 1: 62H,00H,3BH,1BH,A5H
- Electronic Volume Set 2: 05H,0FH,3BH,A5H,A5H
- Memory Address Control: 24H,01H,A5H,A5H,A5H
- BPP Select: 22H,02H,A5H,A5H,A5H
- Gamma Set 4bpp Positive 1: 91H,00H,21H,23H,24H
- Gamma Set 4bpp Positive 2: 92H,27H,28H,29H,2AH
- Gamma Set 4bpp Positive 3: 93H,2BH,2CH,2DH,2EH
- Gamma Set 4bpp Positive 4: 94H,30H,31H,32H,3FH
- Gamma Set 4bpp Negative 1: 99H,00H,21H,23H,26H
- Gamma Set 4bpp Negative 2: 9AH,27H,28H,29H,2AH
- Gamma Set 4bpp Negative 3: 9BH,2BH,2CH,2DH,2EH
- Gamma Set 4bpp Negative 4: 9CH,30H,35H,3BH,35H
- Sleep Out: 12H,A5
- Display On: 15H,A5

8.7 DISPLAY DATA RAM

Page address		0	1	2	..	637	638	639	normal	Column address
normal	invert	639	638	637	..	2	1	0	invert	
0	159	D[0:3]	D[0:3]	D[0:3]	..	D[0:3]	D[0:3]	D[0:3]	<b>G0</b>	
		D[4:7]	D[4:7]	D[4:7]	..	D[4:7]	D[4:7]	D[4:7]	<b>G1</b>	
1	158	D[0:3]	D[0:3]	D[0:3]	..	D[0:3]	D[0:3]	D[0:3]	<b>G2</b>	
		D[4:7]	D[4:7]	D[4:7]	..	D[4:7]	D[4:7]	D[4:7]	<b>G3</b>	
158	1	D[0:3]	D[0:3]	D[0:3]	..	D[0:3]	D[0:3]	D[0:3]	<b>G316</b>	
		D[4:7]	D[4:7]	D[4:7]	..	D[4:7]	D[4:7]	D[4:7]	<b>G317</b>	
159	0	D[0:3]	D[0:3]	D[0:3]	..	D[0:3]	D[0:3]	D[0:3]	<b>G318</b>	
		D[4:7]	D[4:7]	D[4:7]	..	D[4:7]	D[4:7]	D[4:7]	<b>G319</b>	
<b>Source</b>		<b>S0</b>	<b>S1</b>	<b>S2</b>	..	<b>S637</b>	<b>S638</b>	<b>S639</b>	<b>Gate</b>	

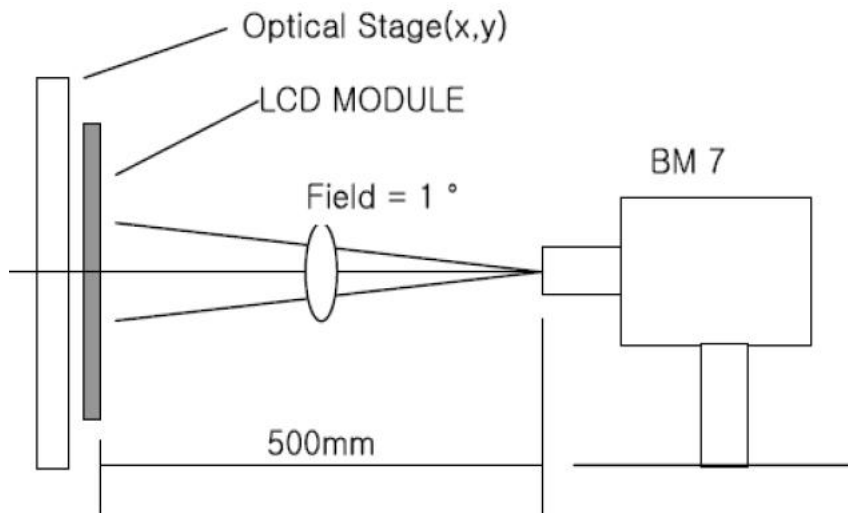
9. Optical Specification

Item	Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio	CR	$\theta=0^\circ$	--	400	--	--	Note1 Note2
Response Time	Tr	Ta= 25°C	--	20	--	ms	Note1
	+Tf		--	10	--	ms	Note3
View Angles	$\theta T$	CR $\geq 2$	-	60	-	Degree	Note 4
	$\theta B$		-	50	-		
	$\theta L$		-	60	-		
	$\theta R$		-	60	-		
Luminance				1400		cd/m <sup>2</sup>	Note 5

Note 1: Definition of optical measurement system.

Temperature = 25°C(±3°C)

LED back-light: ON, Environment brightness < 150 lx

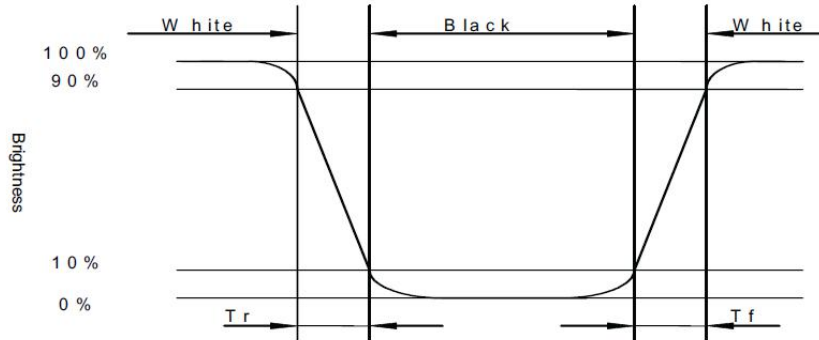


Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

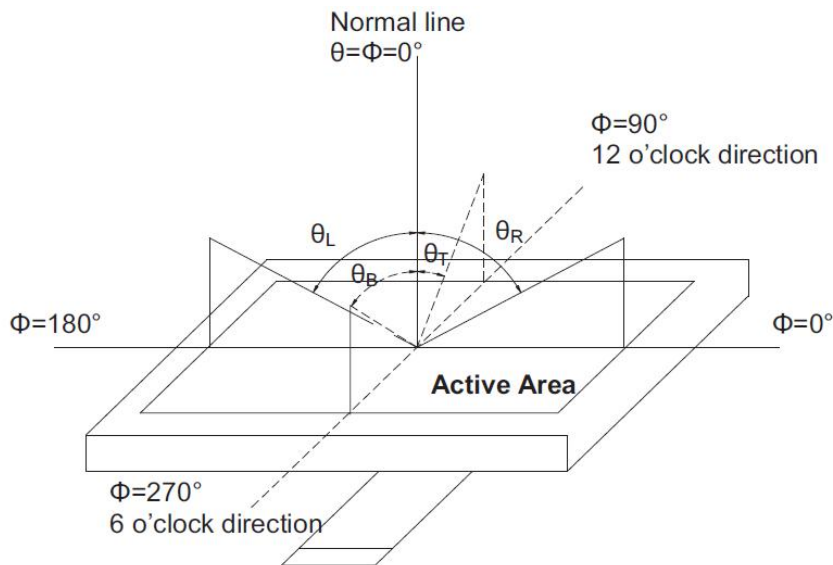
**Note 3: Response time is defined as follow:**

Response time is the time required for the display to transition from black to white (Rise Time,  $T_r$ ) and from white to black (Decay Time,  $T_f$ ).



**Note 4: Viewing angle range is defined as follow:**

Viewing angle is measured at the center point of the LCD.



**Note 5: Luminance is defined as follow:**

Luminance is defined as the brightness of all pixels "White" at the center of display area on optimum contrast.

10. Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Operation Temp	Ts=+70°C, 240hrs	Per table in below
2	Low Operation Temp	Ta=-20°C, 240hrs	Per table in below
3	High Temp Storage	Ta=+80°C, 240hrs	Per table in below
4	Low Temp Storage	Ta=-30°C, 240hrs	Per table in below
5	High Temp & High Humidity Storage	Ta=+60°C, 90% RH 96 hours	Per table in below (polarizer discoloration is excluded)
6	Thermal Shock (Non-operation)	-30°C 30 min~+80°C 30 min, Change time:5min, 100 Cycles	Per table in below
7	ESD (Operation)	+/-2KV, Human Body Mode, 100pF/1500	Per table in below
8	Vibration (Non-operation)	Frequency range : 10~55Hz Stroke: 1.5mm Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X. Y. Z. (6 hours for total).	Per table in below
9	Shock (Non-operation)	60G 6ms, ±X,±Y,±Z 3times, for each direction	Per table in below
10	Package Drop Test	Height:60 cm, 1 corner, 3 edges, 6 surfaces	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the LCD Panel
Alignment of LCD Panel	No Bubbles in the LCD Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

## 11. Precautions for Use of LCD Modules

### 11.1 Safety

The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

### 11.2 Handling

- A. The LCD and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
- B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
- C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
- D. Provide a space so that the panel does not come into contact with other components.
- E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
- F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
- G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
- H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

### 11.3 Static Electricity

- A. Ground soldering iron tips, tools and testers when they are in operation.
- B. Ground your body when handling the products.
- C. Power on the LCD module before applying the voltage to the input terminals.
- D. Do not apply voltage which exceeds the absolute maximum rating.
- E. Store the products in an anti-electrostatic bag or container.

### 11.4 Storage

- A. Store the products in a dark place at  $+25^{\circ}\text{C} \pm 10^{\circ}\text{C}$  with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
- B. Storage in a clean environment, free from dust, active gas, and solvent.

### 11.5 Cleaning

- A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
- B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

### 11.6 Cautions for installing and assembling

Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.

