ALL SHORE INDUSTRIES

ASI-T-270EA28N/D

Item	Contents	Unit
Size	2.7	inch
Resolution	960(Delta RGB)x 240	/
Interface	8-bit RGB /8-bit Dummy RGB/CCIR656/601	/
Technology type	a-Si TFT	/
Pixel pitch	0.16875x0.16875	mm
Pixel Configuration	R.G.B. Delta	
Outline Dimension (W x H x D)	63.50x46.60x2.60	mm
Active Area	54.00 x 40.50	mm
Display Mode	Transmissive, Normally white	/
Viewing Direction	12 O'clock	/
Backlight Type	LED	/
Driver IC	HX8268-C	/
Weight	16.3	g

Record of Revision

Date	Revision No.	Summary
2016-08-14	1.0	Rev 1.0 was issued

1. Scope

This data sheet is to introduce the specification of ASI-T-270EA28N/D active matrix TFT module. It is composed of a color TFT-LCD panel, driver ICs, FPC and a backlight unit. The 2.7″ display area contains 960 (Delta RGB) x 240 pixels.

2. Application

Digital equipments which need color display, Digital Camera, mobile phone, mobile navigator/video systems.

3. General Information

Item	Contents	Unit
Size	2.7	inch
Resolution	960(Delta RGB)x 240	/
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Technology type	a-Si TFT	/
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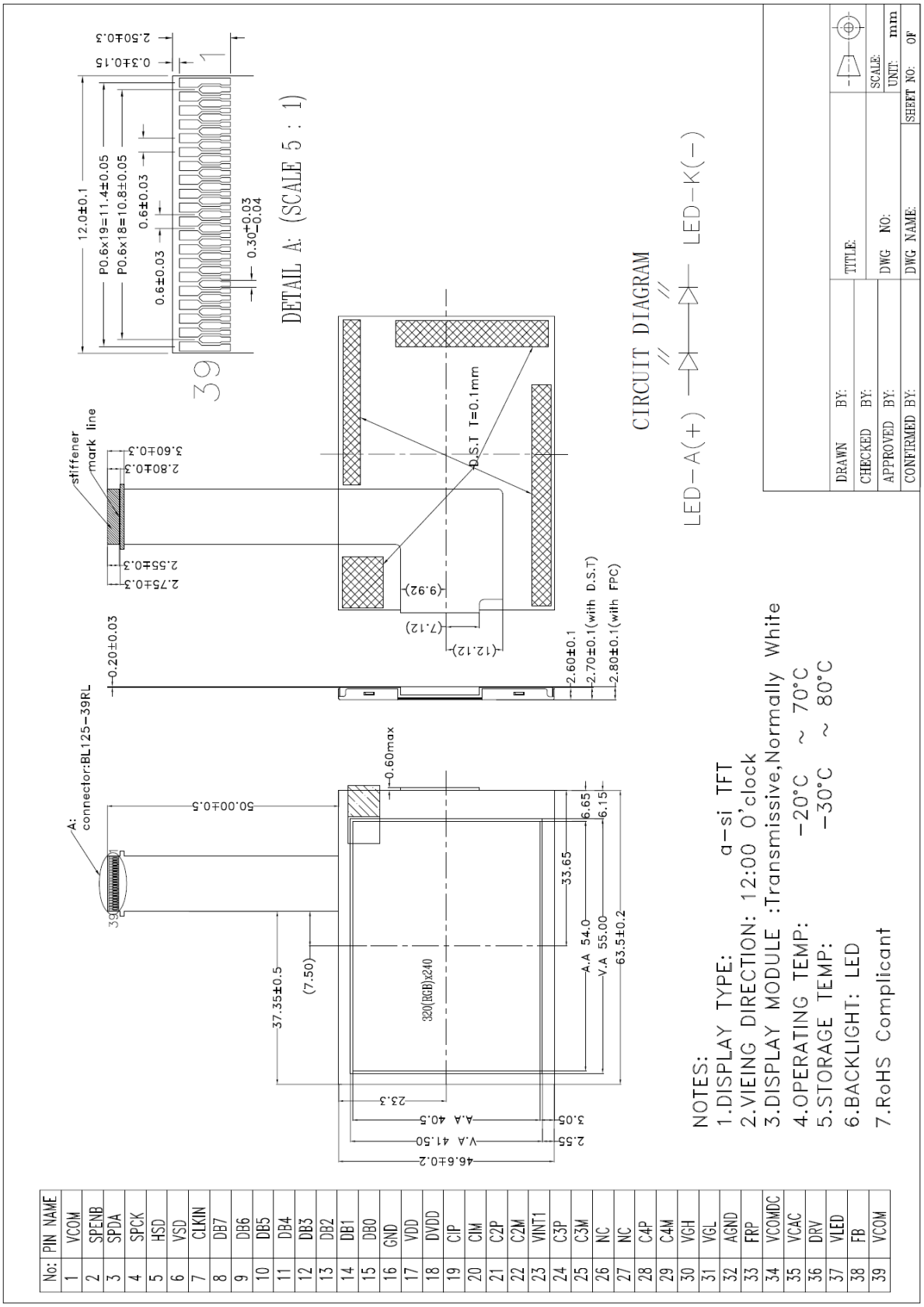
Pixel Configuration	R.G.B. Delta	
Outline Dimension (W x H x D)	63.50x46.60x2.60	mm
Active Area	54.00 x 40.50	mm
Display Mode	Transmissive, Normally white	/
Viewing Direction	12 O'clock	/
Backlight Type	LED	/
Driver IC	HX8268-C	/
Weight	16.3	g

4. Outline Drawing



No:	PIN NAME
1	VCOM
2	SPENB
3	SPDA
4	SPCK
5	HSD
6	VSD
7	CLKIN
8	DB7
9	DB6
10	DB5
11	DB4
12	DB3
13	DB2
14	DB1
15	DB0
16	GND
17	VDD
18	DVDD
19	CIP
20	CIM
21	C2P
22	C2M
23	VINT1
24	C3P
25	C3M
26	NC
27	NC
28	C4P
29	C4M
30	VGH
31	VGL
32	AGND
33	FRP
34	VCOMDC
35	VCAC
36	DRV
37	VLED
38	FB
39	VCOM

5. Interface signals

No	Symbol	I/O	Description	Remark
1	VCOM	I	Panel common voltage	
2	SPENB	I	SPI enable	
3	SPDA	I/O	SPI data input/output	
4	SPCK	I	SPI clock input	
5	HSD	I	Horizontal sync input	
6	VSD	I	Vertical sync input	
7	CLKIN	I	Data clock input	
8	DB7	I	Data input; MSB	
9	DB6	I	Data input	
10	DB5	I	Data input	
11	DB4	I	Data input	
12	DB3	I	Data input	
13	DB2	I	Data input	
14	DB1	I	Data input	
15	DB0	I	Data input; LSB	
16	GND	P	Power ground	
17	VDD	P	Supply power	
18	DVDD	C	Power setting capacitor connect pin	
19	C1P	C	Capacitor for charge pump	
20	C1M	C	Capacitor for charge pump	
21	C2P	C	Capacitor for charge pump	
22	C2M	C	Capacitor for charge pump	
23	VINT1	C	Power setting capacitor connect pin	
24	C3P	C	Capacitor for charge pump	
25	C3M	C	Capacitor for charge pump	
26	NC	-	No connection	
27	NC	-	No connection	
28	C4P	C	Capacitor for charge pump	
29	C4M	C	Capacitor for charge pump	
30	VGH	C	Power setting capacitor connect pin	
31	VGL	C	Power setting capacitor connect pin	
32	AGND	P	Power ground	
33	FRP	O	Frame Polarity output for VCOM	
34	VCOMDC	O	VCOM DC output in	
35	VCAC	C	Power setting capacitor connect pin	
36	DRV	O	VLED boost driving signal	
37	VLED	P	LED power anode	
38	FB	P	LED power cathode	
39	VCOM	I	Panel common voltage	

Note: Matching Connector: FH26-39S-0.3SHW

I/O Definition: I-----Input O---Output , P----Power(Ground) NC---No connection

6. Absolute maximum Ratings

6.1. Electrical Absolute max. ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Supply Voltage	VDD	-0.3	5.0	V	
Input signal voltage	DB0~DB7,VCOM,SPENB,SPDA,SPCK, HSD,VSD,CLKIN	-0.3	VDD +0.3	V	

6.2. Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-20	70	℃	
Storage Temperature	TSTG	-30	80	℃	

6.3. LED Backlight Absolute max. ratings

Item	Symbol	MIN	MAX	Unit	Remark
LED Forward Current	ILED	--	25	mA	One LED

7. Electrical Specifications

7.1 Electrical characteristics

GND=0V, Ta=25℃

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Supply Voltage		VDD	3.0	3.3	3.6	V	
Input Signal Voltage	High Level	VIH	0.7×VDD	-	VDD	V	
	Low Level	VIL	GND	-	0.3×VDD	V	
Output Signal Voltage	High Level	VOH	VDD-0.4	-	VDD	V	
	Low Level	VOL	GND	-	0.4	V	
(Panel+ LSI) Power Consumption		Normal Mode	-	6.78	-	mA	CLK 27MHz
		Standby Mode	-	22	-	uA	

7.2 LED Backlight

Ta=25℃

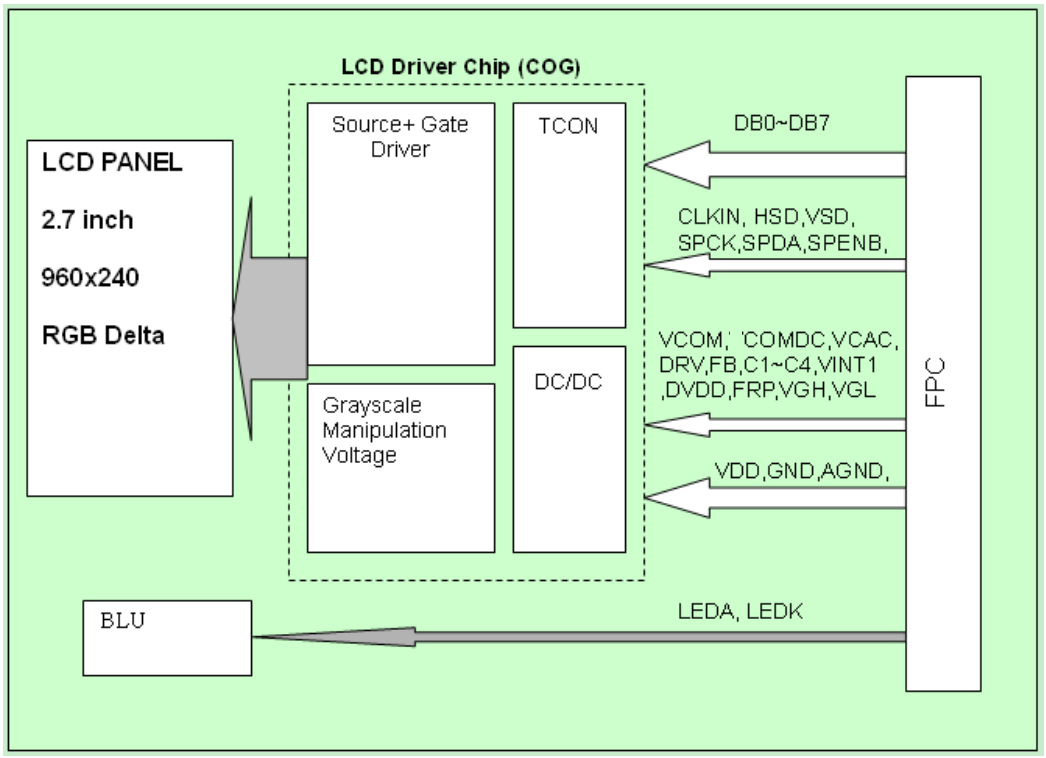
Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	IF		20		mA	For one LED Note 1,2,3
Forward Voltage	VF	2.9	3.2	3.5	V	
Power Consumption	--		128		mW	
Operating Life Time	--	10000	20000		Hrs	

Note 1: Backlight LED Circuit:

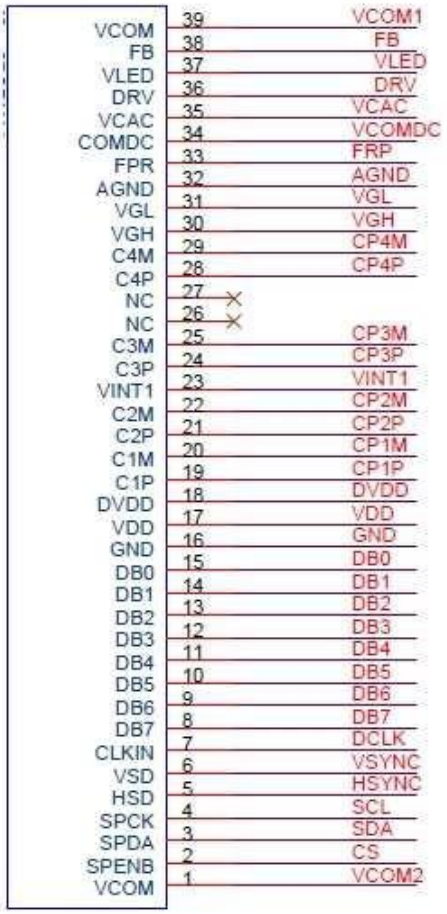
Note 2: One LED : IF =20mA, VF=3.2V

Note 3 : IF is defined for one channel LED.
Optical performance should be evaluated at Ta = 25 ℃ only.
If LED is driven by high current, high ambient temperature & humidity condition.
The life time of LED will be reduced.
Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

7.3 Block Diagram



7.4 Application Circuit



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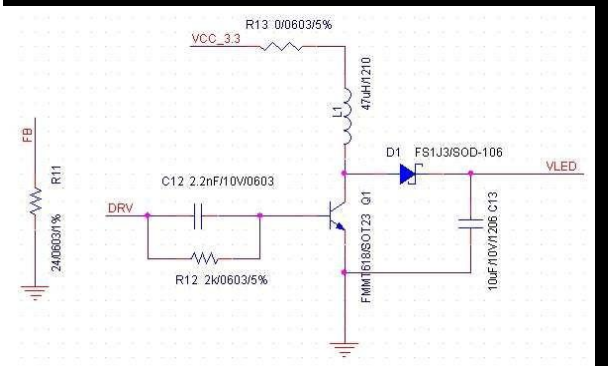
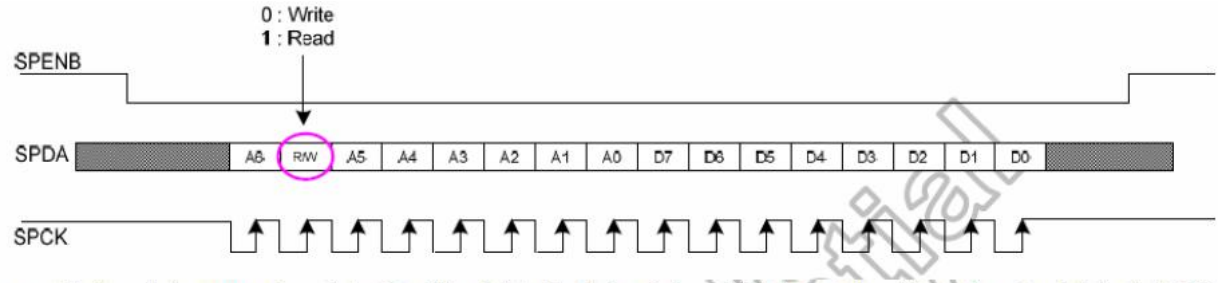


Recommend value of capacitor

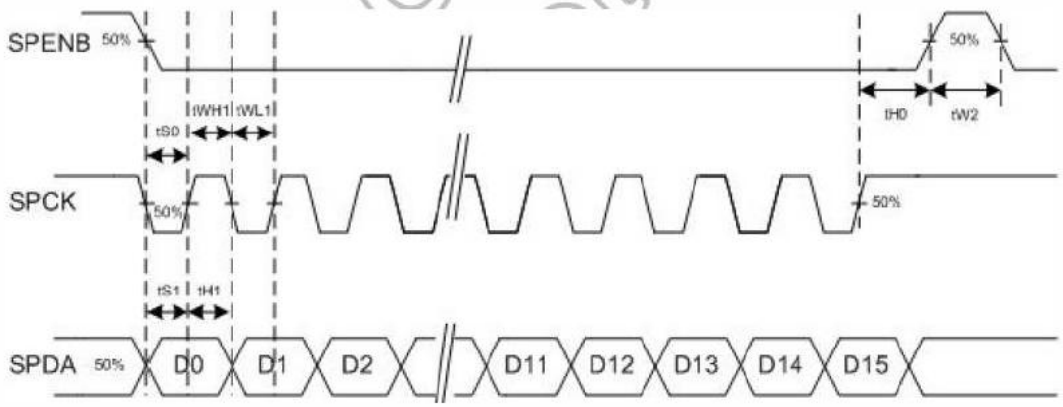
Pad name	CAP (μF)	Pad name	CAP (μF)
C1P	1~2.2uF/6.3V	VDD	1uF/6.3V
C1M		DVDD	1uF/6.3V
C2P	1uF/6.3V	VINT	2.2uF/10V
C2M		VGH	2.2uF/25V
C3P	1uF/10V	VGL	2.2uF/16V
C3M		VCAC	2.2uF/6.3V
C4P	1uF/16v	FRP-VCOMDC	2.2uF/6.3V
C4M			

8. Command/AC Timing

8.1 3-Wire Serial Control Interface



- Each serial command consists of 16 bits of data that is loaded one bit a time at the rising edge of serial clock SPCK. Command loading operation starts from the falling edge of SPENB and is completed at the next rising edge of SPENB.
- The serial control block is operational after power on reset, but commands are established by the VSD signal. If command is transferred multiple times for the same register, the last command before the VSD signal is valid.
- If less than 16 bits of SPCK are input while SPENB is low, the transferred data is ignored.
- If 16 bits or more of SPCK are input while SPENB is low, the last 16 bits of transferred data before the rising edge of SPENB pulse are valid data.
- Serial block operates with the SPCK clock
- Serial data can be accepted in the power save mode.



PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
SPENB input setup time	tS0	50			ns
SPDA input setup time	tS1	50			ns
SPENB input hold time	tH0	50			ns
SPDA input hold time	tH1	50			ns
SPCK pulse high width	tWH1	50			ns
SPCK pulse low width	tWL1	50			ns
SPENB pulse high width	tW2	400			ns

8.2 Register Table

Register	Register Address								Register Data (default)							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R00h	0	0	0	0	0	0	0	0	Y_CbCr	CCIR601			VCOM_AC			
									0	0	x		1	0	1	1
R01h	0	0	0	0	0	0	0	1	VCDCEN		VCOM_DC					
									1	x	0	1	1	1	0	0
R03h	0	0	0	0	0	0	1	1	Brightness							
									0	1	0	0	0	0	0	0
R04h	0	0	0	0	0	1	0	0	Narrow	YUV	SEL		NTSC/PAL		VDIR	HDIR
									0	0	0	0	1	0	1	1
R05h	0	0	0	0	0	1	0	1	DRV_FREQ	GRB	PWM_DUTY			VGH/L_EN	LED_EN	
									0	1	0	1	1	1	1	x
R06h	0	0	0	0	0	1	1	0	HBLK_EN	LED_Current			VBLK			
									0	0	0	1	0	1	0	1
R07h	0	0	0	0	0	1	1	1	HBLK							
									0	1	0	0	0	1	1	0
R08h	0	0	0	0	1	0	0	0	BL_DRV							
									0	0	x					
R0Bh	0	0	0	0	1	0	1	1	REGSEL							
									0	x						
R0Ch	0	0	0	0	1	1	0	0	PAIR		DESEL	CbCr	DEpol	VDpol	HDpol	CLKINpol
									0	0	0	0	0	1	1	0
R0Dh	0	0	0	0	1	1	0	1	CONTRAST							
									0	1	0	0	0	0	0	0
R0Eh	0	0	0	0	1	1	1	0	SUB-CONTRAST_R							
									x	1	0	0	0	0	0	0
R0Fh	0	0	0	0	1	1	1	1	SUB-BRIGHTNESS_R							
									x	1	0	0	0	0	0	0
R10h	0	0	0	1	0	0	0	0	SUB-CONTRAST_B							
									x	1	0	0	0	0	0	0
R11h	0	0	0	1	0	0	0	1	SUB-BRIGHTNESS_B							
									x	1	0	0	0	0	0	0
R12h	0	0	0	1	0	0	1	0	TRMEN							
									0	0	0	0	0	0	0	0
R13h	0	0	0	1	0	0	1	1								ENTRY_EN
												x				0
R16h	0	0	0	1	0	1	1	0						GAMMA2.2		
											x			1	x	
R17h	0	0	0	1	0	1	1	1		GMA_VP16					GMA_VP8	
									x	1	0	0	x	1	0	0
R18h	0	0	0	1	1	0	0	0		GMA_VP50					GMA_VP32	
									x	1	0	1	x	1	0	0
R19h	0	0	0	1	1	0	0	1		GMA_VP96					GMA_VP72	
									x	1	0	0	x	0	1	1
R1Ah	0	0	0	1	1	0	1	0		GMA_VP120					GMA_VP110	
									x	1	0	1	x	1	0	0
R2Bh	0	0	1	0	1	0	1	1								STB
												x				0
R2Fh	0	0	1	0	1	1	1	1	VGH_SEL			CF_SEL	LC_TYPE		SOPC	
									0	1	1	0	1	1	0	1
R3Ch	0	0	0	1	0	1	1	1	x	GMA_VP127			x		GMA_VP0	
										0	1	1		1	0	0
R3Dh	0	0	0	1	1	0	0	0		GMA_VPN127					GMA_VN0	
									x	0	1	0	x	1	0	1
R3Eh	0	0	0	1	1	0	0	1		GMA_VN16					GMA_VN8	
									x	1	0	0	x	1	0	0
R3Fh	0	0	0	1	1	0	1	0		GMA_VN50					GMA_VN32	
									x	1	0	1	x	1	0	0
R40h	0	0	0	1	1	0	0	0		GMA_VN96					GMA_VN72	
									x	1	0	0	x	0	1	1
R41h	0	0	0	1	1	0	0	1		GMA_VN120					GMA_VN110	
									x	1	0	1	x	1	0	0
R4Fh	0	0	0	1	1	1	1	1					ID			
									x	0	0	0	1	0	0	1
R55h	1	0	0	1	0	1	0	1	INV_SEL	DAT_INV						
									x	0	0			x		
R57h	1	0	0	1	0	1	1	1	VGHL_ENB							
									x	0				x		
R5Ah	1	0	0	1	1	0	1	0							VGL_SEL	
									x					0	1	0

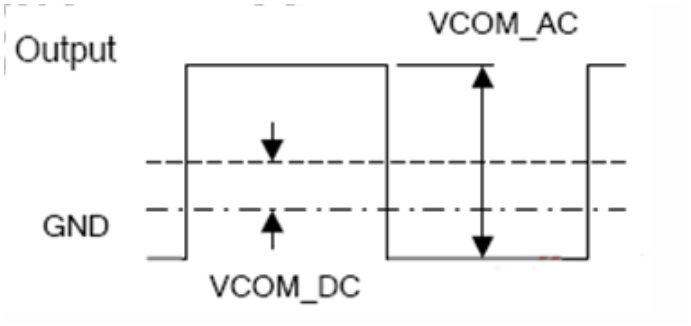
8.3 3-Wire Register Description

R00h:Data Format & VCOM AC Setting

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	Y_Cb Cr	CCIR601	-	-	VCOM_AC			
Initial setting value (default)								0	0	-	-	1	0	1	1

VCOM_AC : Common voltage AC level selection

D3	D2	D1	D0	LV LC (V)	NV LC-1 (V)	NV LC-2 (V)
0	0	0	0	3.7	4.0	5.0
0	0	0	1	3.8	4.1	5.1
0	0	1	0	3.9	4.2	5.2
0	0	1	1	4.0	4.3	5.3
0	1	0	0	4.1	4.4	5.4
0	1	0	1	4.2	4.5	5.5
0	1	1	0	4.3	4.6	5.6
0	1	1	1	4.4	4.7	5.7
1	0	0	0	4.5	4.8	5.8
1	0	0	1	4.6	4.9	5.9
1	0	1	0	4.7	5.0	6.0
1	0	1	1	4.8 (**default**)	5.1 **(default)**	6.1 (**default**)
1	1	0	0	4.9	5.2	6.2
1	1	0	1	5.0	5.2	6.2
1	1	1	0	5.1	5.2	6.2
1	1	1	1	5.2	5.2	6.2



CCIR601 : CCIR601 input timing selection

CCIR601	Function
0	Disable CCIR601. (Default)
1	Enable CCIR601. (please refer to the table of R4(SEL) for detail description)

Y_CbCr : Y & CbCr exchange position (only valid for 8-bit input YUV640 / YUV720)

Y_CbCr	CbCr (R12[4])															
	0								1							
0	Cb0	Y0	Cr0	Y1	Cb2	Y2	Cr2	Y3	Cr0	Y0	Cb0	Y1	Cr2	Y2	Cb2	Y3
1	Y0	Cb0	Y1	Cr0	Y2	Cb2	Y3	Cr2	Y0	Cr0	Y1	Cb0	Y2	Cr2	Y3	Cb2

R01h:VCOM DC Setting

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	VCDCE	-	VCOM_DC					
Initial setting value (default)								1	-	1	0	1	1	0	0

VCOM_DC: Common voltage DC level selection (20mV/step)

D[5:0]	VCOM DC offset
00h	0.24
:	:
1Ch	**0.8** (**default**)
3Fh	1.5

VCDCE : VCOM DC enable control

VCDCE	Function
0	VCOM_DC function disabled. The VCOMDC pin is disabled
1	VCOM_DC function enabled. The VCOMDC voltage follows VCOM_DC setting. (default)

R03h:Whole Brightness Adjustment

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	1	Brightness							
Initial setting value (default)								0	1	0	0	0	0	0	0

Brightness : Adjust RGB Brightness

D7~D0	Brightness gain
00h	Dark(-64)
40h	Center(0)(default)
FFh	Bright(+191)

Setting accuracy 1bit/step

R04h:

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	0	Narrow	YUV	SEL		NTSC/PAL		VDIR	HDIR
Initial setting value (default)								0	0	0	0	1	0	1	1

HDIR : Shift registers of source driver direction selection

D0	HDIR Function
0	Shift from right to left. Y0 Y1 … Yn-1 Yn
1	Shift from left to right. Y0 Y1 … Yn-1 Yn (Default)

VDIR : Gate driver output direction selection

D1	VDIR Function
0	Shift from down to up. L0 L1 … L239 L240
1	Shift from up to down. L0 L1 … L239 L240 (Default)

NTSC/ PAL : NTSC or PAL input mode selection

D3	D2	NTSC/PAL Mode
0	0	PAL.
0	1	NTSC.
1	x	Auto detection. (Default)

SEL : Input data timing format selection

CCIR601	YUV	SEL		Input Timing format
		D5	D4	
0	0	0	0	8-bit RGB. (Default)
0	0	0	1	8-bit Dummy RGB 320 x 240.
0	0	1	x	8-bit Dummy RGB 360 x 240.
0	1	x	x	CCIR656.
1	1	0	x	YUV 640.
1	1	1	0	YUV 720.

YUV : YUV(CCIR656) or RGB input selection

D6	Data format
0	RGB input. (Default)
1	CCIR656/YUV640/YUV720 input.

Narrow : Normal display and Narrow display selection

D7	Function
0	Normal display. (Default)
1	Narrow display

Note: Narrow function was not supporting 8-bit RGB and 24-bit RGB input mode.

Narrow = 0

Narrow = 1

Figure: **The Narrow function**

R05h:

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	1	DRV_RREQ	GRB	PWM_DUTY			VGH/L_EN	LED_EN	-
Initial setting value (default)								0	1	0	1	1	1	1	-

LED_EN : Shut down for back light power converter

D1	LED_EN Function
0	The back light power converter is off.
1	The back light power converter is controlled by STB's power on/off sequence. (Default)

VGH/L_EN : Shut down for VGH/VGL charge pump

D1	VGH/L_EN Function
0	VGH/VGL charge pump is off.
1	VGH/VGL charge pump is controlled by STB's power on/off sequence. (Default)

PWM_DUTY : PWM duty cycle selection for back light power convert

PWM_DUTY			Function
D5	D4	D3	PWM duty cycle
0	0	0	20%
0	0	1	26%
0	1	0	32%
0	1	1	38% (Default)
1	0	0	44%
1	0	1	50%
1	1	0	56%
1	1	1	62%

GRB : Global reset

D6	GRB Function
0	Reset all registers to default value.
1	Normal operation. (Default)

DRV_FREQ : DRV signal frequency setting

D7	GRB Function
0	High frequency (Default)
1	Low frequency

R06h :

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	1	0	HBLK_EN	LED_Current		VBLK				
Initial setting value (default)								0	0	0	1	0	1	0	1

VBLK : Vertical blanking setting for 8-bit RGB , 8-bit Dummy RGB & CCIR656

For 8-bit RGB, 8-bit Dummy RGB, CCIR656, YUV640 and YUV720 NTSC mode, parallel RGB mode(PSEL=0)

D[4:0]	Function	Unit
00h~03h	3	H(Line)
04h	4	
15h	21(Default)	
1Fh	31	

For 8-bit Dummy RGB, CCIR656, YUV640 and YUV720 PAL mode. (Vertical blanking+3)

D[4:0]	Function	Unit
00h	3	H(Line)
04h	7	
15h	24(Default)	
1Fh	34	

LED_CURRENT : LED current adjustable for DC-DC feedback threshold voltage

D[6:5]	Feedback Threshold Voltage
00	0.6 V. (default)
01	0.75V.
10	0.45V.
11	0.3V.

HBLK_EN : HBLK function enable

D[7]	HBLK EN Function
0	Disable(**default**)
1	Enable

R07h:Horizontal Blanking Setting

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	1	1	HBLK							
Initial setting value (default)								0	1	0	0	0	1	1	0

HBLK : Horizontal blanking setting

HBLK_EN	D7~D0	HBLK	Unit	NTSC/PAL Mode
X	32h~45h	50~69	CLKIN	8-bit RGB.
X	46h	70		
X	47h~FFh	71~255		
0	X	241		8-bit Dummy RGB.
1	00h~03h	3		
	04h~FFh	4~255		
0	XXh	240		YUV640, YUV720.
1	00h~03h	3		
	04h~FFh	4~255		
0	X	61		Parallel RGB
1	04h~3Fh~	4~63		

R08h : Backlight Driving Capacity Setting

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	0	BL_DRV		-	-	-	-	-	-
Initial setting value (default)								0	0	-	-	-	-	-	-

BL_DRV : Backlight driving capability setting

D7	D6	BL_DRV capability
0	0	Normal capability. (Default)
0	1	2 times the Normal capability.
1	0	4 times the Normal capability.
1	1	8 times the Normal capability.

R0Bh : MTP

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	1	REGSEL	-	-	-	-	-	-	-
Initial setting value (default)								0	-	-	-	-	-	-	-

REGSEL MTP function control register

D7	REGSEL Function
0	VCOM_DC[5:0] is read from MTP memory. (Default)
1	VCOM_DC[5:0] is switch to the 3-wire register memory when user want to adjust the VCOMDC level for

R0Ch:

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	0	PAIR		SESEL	CbCr	DEpol	VDpol	HDpol	CLKINpol
Initial setting value (default)								0	0	0	0	0	1	1	0

CLKINpol CLKIN polarity selection

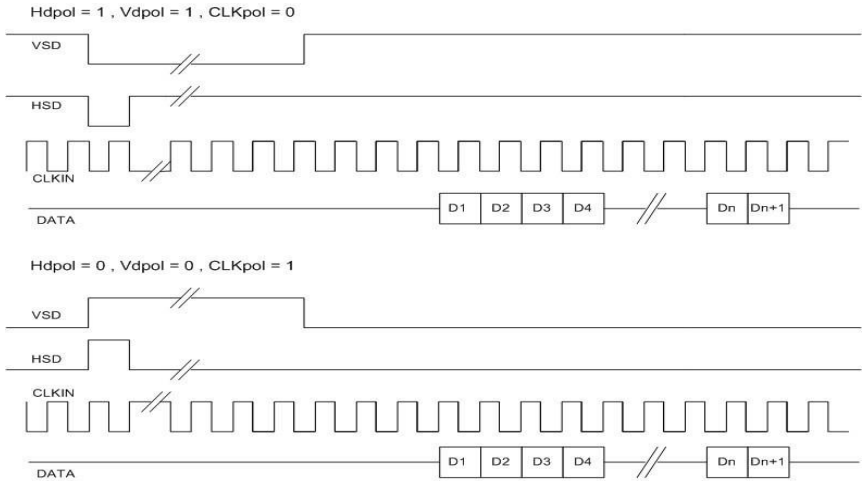
D0	CLKINpol Function
0	Positive polarity. (Default)
1	Negative polarity

HDpol HSD polarity selection

D1	HDpol Function
0	Positive polarity.
1	Negative polarity. (Default)

VDpol VSD polarity selection

D2	VDpol Function
0	Positive polarity.
1	Negative polarity. (Default)



DEpol DEN polarity selection

D3	DEpol Function
0	Positive polarity (Default)
1	Negative polarity

CbCr Cb & Cr exchange position (valid for CCIR656 and YUV640/YUV720)

D4	CbCr Function
0	Cb Y Cr. (Default)
1	Cr Y Cb

DESEL DE Mode selection

D5	DESEL Function
0	HV mode selected. (Default)
1	DE mode selected.

DESEL only controls the HV and DE mode at 8-bit RGB, 8-bit Dummy RGB and Parallel Mode.

PAIR Vertical start time of Odd/Even Frame

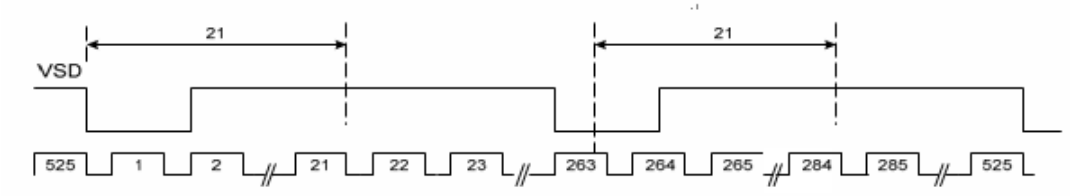
PAIR		VBLK	Unit
D7	D6	ODD/EVEN	
-	0	21/21. (Default)	H (Line)
-	1	21/20.	

For 8-bit RGB / 8-bit Dummy RGB NTSC / 8-bit Dummy RGB PAL, parallel RGB mode(PSEL=0)
The typical value of VBLK of 8-bit Dummy RGB PAL(24 H) is different than 8-bit RGB/8-bit Dummy RGB NTSC(21H)

PAIR		VBLK	Unit
D7	D6	ODD/EVEN	
0	0	21/21. (Default)	H (Line)
0	1	21/22.	
1	0	22/21.	
1	1	22/22.	

For CCIR656/YUV640/YUV720 NTSC/PAL
The typical value of VBLK of CCIR656 PAL(24 H) is different than CCIR656 NTSC(21H).

Note: Vertical blanking must be adjusted base on the input data.



R0Dh:Whole Contrast Adjustment

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	1	CONTRAST							
Initial setting value (default)								0	1	0	0	0	0	0	0

CONTRAST : RGB contrast level setting , the gain changes (1/64) / bit

D[7:0]	Contrast gain
00h	0
40h	1 (Default)
FFh	3.984

R0Eh:R Contrast Adjustment

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	1	0	-	SUB-CONTRAST_R						
Initial setting value (default)								-	1	0	0	0	0	0	0

SUB-CONTRAST_R : Red sub-pixel contrast level setting, the gain changes (1/256)/bit

D[6:0]	R Contrast gain
00h	0.75
40h	1 (Default)
7Fh	1.246

R0Fh:R Brightness Adjustment

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	1	1	-	SUB-BRIGHTNESS_R						
Initial setting value (default)								-	1	0	0	0	0	0	0

SUB-BRIGHTNESS_R Red sub-pixel brightness level setting, setting accuracy:1 step/bit

D[6:0]	R Brightness gain
00h	DARK (-64)
40h	Center (0) (Default)
7Fh	Bright (+63)

R10h:B Contrast Adjustment

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	0	-	SUB-CONTRAST_B						
Initial setting value (default)								-	1	0	0	0	0	0	0

sUB-CONTRAST_B Blue sub-pixel contrast level setting, the gain changes (1/256)/bit

D[6:0]	B Contrast gain
00h	0.75
40h	1 (Default)
7Fh	1.246

R11h:B Brightness Adjustment

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	1	-	SUB-BRIGHTNESS_B						
Initial setting value (default)								-	1	0	0	0	0	0	0

SUB-BRIGHTNESS_B Blue sub-pixel brightness level setting, setting accuracy:1 step/bit

D6~D0	B Brightness gain
00h	DARK (-64)
40h	Center(0) (Default)
7Fh	Bright (+63)

R12h:Instruction for OTP

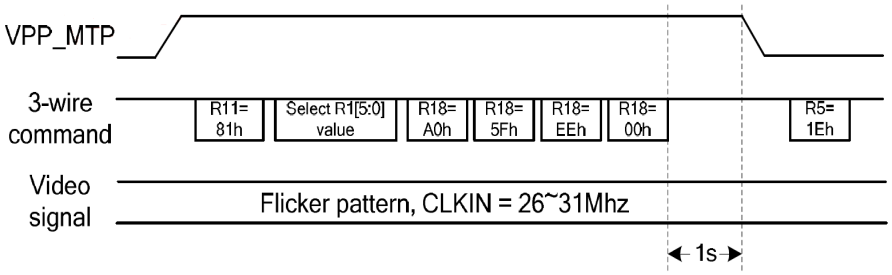
Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	1	0	TRMEN							
Initial setting value (default)								0	0	0	0	0	0	0	0

TRMEN VCOM DC Trim Function Control Register

VCOMDC Trim function control register, this IC have build-in MTP memory, at Power-on, IC will auto load the MTP memory to set the VCOMDC level to prevent flick issue.

Operation condition:
1. CLKIN frequency range 26Mhz ~ 31Mhz
2. Apply 7.5V to VPPMTP pin.

Programming procedure:
1. Set REGSEL = 1
2. Adjustment VCOM_DC(R1[5:0]) value, select proper VCOM_DC value
3. Set TRMEN[7:0] as following sequence : **A0h 5Fh EEh 00h**.
4. Hold 1s for MTP control block operation.
5. Set global reset (set R5[6] = 1) and restart the display operation.
6. Check the VCOMDC value.



Note:(1) The Trim Block can be writing only for "3" times.
(2) After finishing TRMEN command do not power off within 1 second.
(3) Trim command exceed the limit may cause the VCOMDC output unknown value.

R13h:Entry Function Control

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	1	1	-	-	-	-	-	-	-	ENTRY_EN
Initial setting value (default)								-	-	-	-	-	-	-	0

ENTRY_EN Entry function control

ENTRY_EN	Function
0	Through mode: Input data must be aligned with the color filter arrangement (default).
1	Alignment mode: Input data must always be the R1, G1, B1,R2, G2,

R16h:Gamma 2.2

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	1	0	-	-	-	-	-	GAMMA2.2	-	-
Initial setting value (default)								-	-	-	-	-	1	-	-

GAMMA2.2 : Select auto or manual gamma setting

D2	Function
0	Manual set gamma by R17h~R1Ah and R3Ch~R41h.
1	Auto set to gamma2.2. (default)

R17h、R18h、R19h、R1Ah:Gamma Point Setting

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	1	1	-	GMA_VP16			-	GMA_VP8		
Initial setting value (default)								-	1	0	0	-	1	0	0
0	0	0	1	1	0	0	0	-	GMA_VP50			-	GMA_VP32		

Initial setting value (default)								-	1	0	1	-	1	0	0
0	0	0	1	1	0	0	1	-	GMA_VP96			-	GMA_VP72		

Initial setting value (default)								-	1	0	0	-	0	1	1
0	0	0	1	1	0	1	0	-	GMA_VP120			-	GMA_VP110		
Initial setting value (default)								-	1	0	1	-	1	0	0

GMA_VP8 Gamma reference voltage VP8;
GMA_VP16 Gamma reference voltage VP16;
GMA_VP32 Gamma reference voltage VP32;
GMA_VP50 Gamma reference voltage VP50;
GMA_VP72 Gamma reference voltage VP72;
GMA_VP96 Gamma reference voltage VP96;
GMA_VP110 Gamma reference voltage VP110;
GMA_VP120 Gamma reference voltage VP120;

Reference point	000	001	010	011	8	101	110	111
VP0	-8 V	-6 V	-4 V	-2 V	Default	+2 V	+4 V	+6 V
VP8	-8 V	-6 V	-4 V	-2 V	Default	+2 V	+4 V	+6 V
VP16	-4 V	-3 V	-2 V	- V	Default	+ V	+2 V	+3 V
VP32	-4 V	-3 V	-2 V	- V	Default	+ V	+2 V	+3 V
VP50	-5 V	-4 V	-3 V	-2 V	- V	Default	+ V	+2 V
VP72	-3 V	-2 V	- V	Default	+ V	+2 V	+3 V	+4 V
VP96	-4 V	-3 V	-2 V	- V	Default	+ V	+2 V	+3 V
VP110	-4 V	-3 V	-2 V	- V	Default	+ V	+2 V	+3 V
VP120	-10 V	-8 V	-6 V	-4 V	-2 V	Default	+2 V	+4 V
VP127	-6 V	-4 V	-2 V	Default	+2 V	+4 V	+6 V	+8 V
VN0	-10 V	-8 V	-6 V	-4 V	-2 V	Default	+2 V	+4 V
VN8	-8 V	-6 V	-4 V	-2 V	Default	+2 V	+4 V	+6 V
VN16	-4 V	-3 V	-2 V	- V	Default	+ V	+2 V	+3 V
VN32	-4 V	-3 V	-2 V	- V	Default	+ V	+2 V	+3 V
VN50	-5 V	-4 V	-3 V	-2 V	- V	Default	+ V	+2 V
VN72	-3 V	-2 V	- V	Default	+ V	+2 V	+3 V	+4 V
VN96	-4 V	-3 V	-2 V	- V	Default	+ V	+2 V	+3 V
VN110	-4 V	-3 V	-2 V	- V	Default	+ V	+2 V	+3 V
VN120	-10 V	-8 V	-6 V	-4 V	-2 V	Default	+2 V	+4 V
VN127	-4 V	-3 V	-2 V	- V	Default	+ V	+2 V	+3 V

Note: (1)For low voltage LC V=40mV V=25mV ,For Normal voltage LC

R2Bh:Standby Mode

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	1	1	-	-	-	-	-	-	-	STB
Initial setting value (default)								-	-	-	-	-	-	-	0

STB Standby (Power saving) mode

STB	Function
0	Standby Mode. (Default)
1	Normal operation.

R2Fh:

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	1	1	1	VGH_SEL			CF_SEL	LC_TYPE		SOPC	
Initial setting value (default)								0	1	1	0	0	0	0	1

VGH_SEL			VGH Voltage
D7	D6	D5	
0	0	0	13V
0	0	1	14V
0	1	0	15V
0	1	1	16V
1	0	0	17V
1	0	1	18V
1	1	0	18V
1	1	1	18V

SOPC Source output driving capability selection

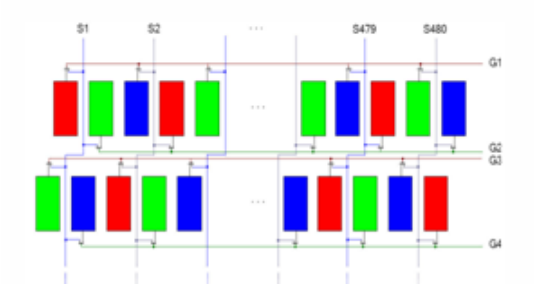
SOPC	Source driver capability
0	-25%.
1	Normal. (default)
2	+25%.
3	+50%.

LC_TYPE : LC type select

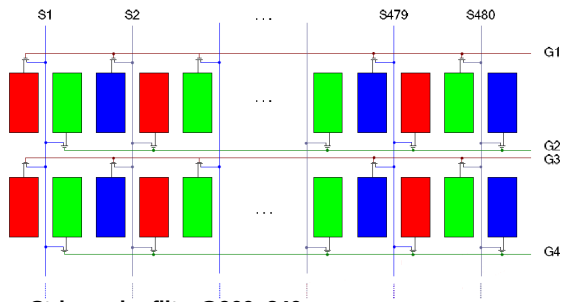
D5	D4	LC_TYPE Function
0	0	Low voltage LC(Default)
0	1	Reserved
1	0	Reserved
1	1	Normal LC

CF_SEL : Color filter selection register

CF_SEL	Function
0	Delta color filter. (Default)
1	Stripe color filter.



Delta color filter@960x240



Stripe color filter@960x240

R55h:Inversion selection

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	1	0	1	-	INV_SEL	DAT_INV	-	-	-	-	-
Initial setting value (default)								-	0	0	-	-	-	-	-

DAT_INV	Inversion
0	Normal data output. (Default)
1	Inversion data output

INV_SEL	Inversion
0	One line inversion. (Default)
1	Column inversion.

R57h:VGHL_ENB

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	1	1	1	VGHL_ENB	-	-	-	-	-	-	-
Initial setting value (default)								0	-	-	-	-	-	-	-

VGHL_ENB	Inversion
0	VGH/VGL charge pump enable (Default)
1	For external VGH/VGL application

R5Ah:VGL_SEL

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	-	0	1	1	0	1	0	-	-	-	-	-	VGL_SEL		
Initial setting value (default)								-	-	-	-	-	0		

VGL_SEL			VGL Voltage
D2	D1	D0	
0	0	0	-8V
0	0	1	-9V
0	1	0	-10V(default)
0	1	1	-11V
1	0	0	-7V
1	0	1	-7V
1	1	0	-11V
1	1	1	-11V

8.4 Data Input Format

8.4.1 Serial 8-bit RGB / 8-bit Dummy RGB / YUV Mode Data format

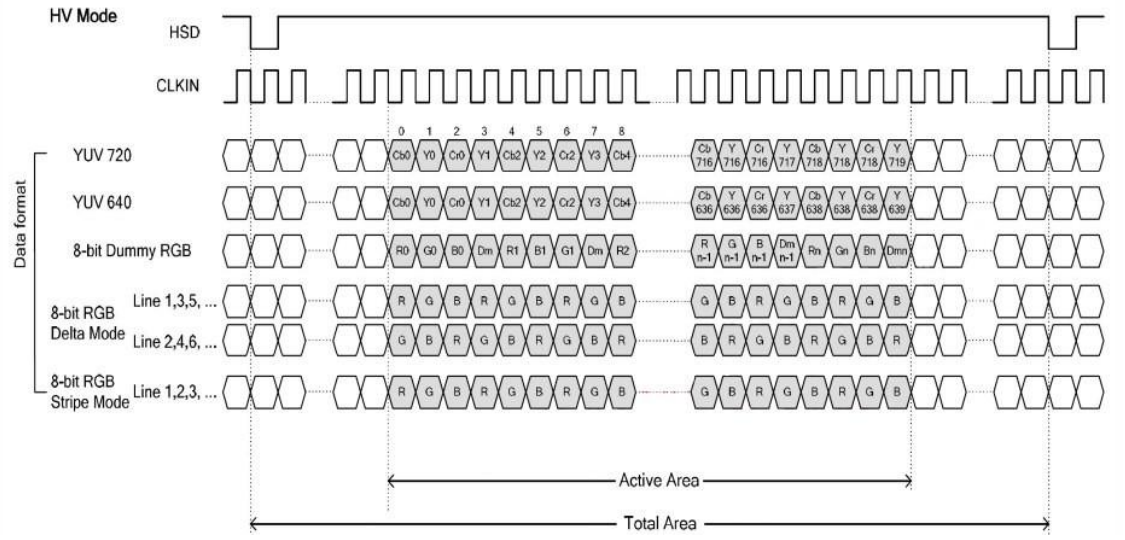


Figure : Serial 8-bit RGB / 8-bit Dummy RGB / YUV Mode Data format HV mode

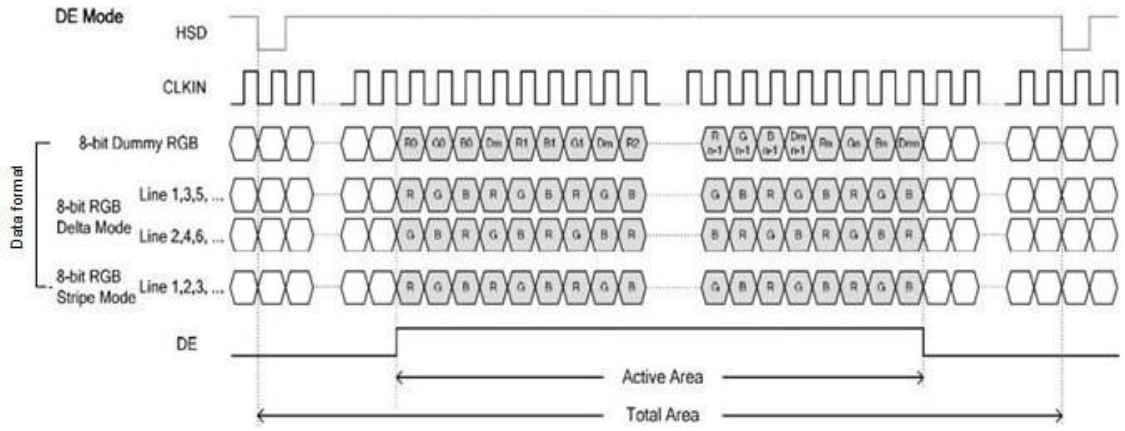


Figure : Serial 8-bit RGB / 8-bit Dummy RGB / YUV Mode Data format DE mode

8.4.2 **Parallel RGB Mode Data format**

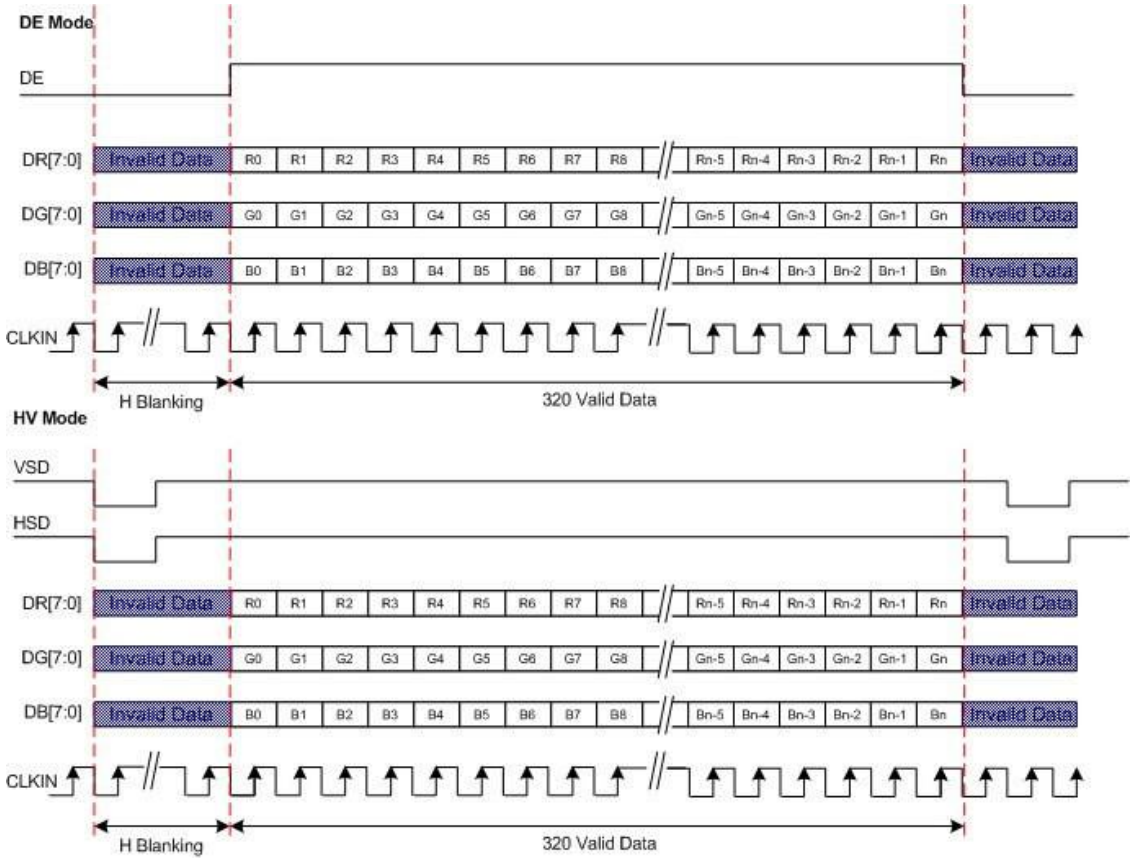


Figure : Parallel RGB Mode Data format

8.4.3 CCIR_656 Mode Data format

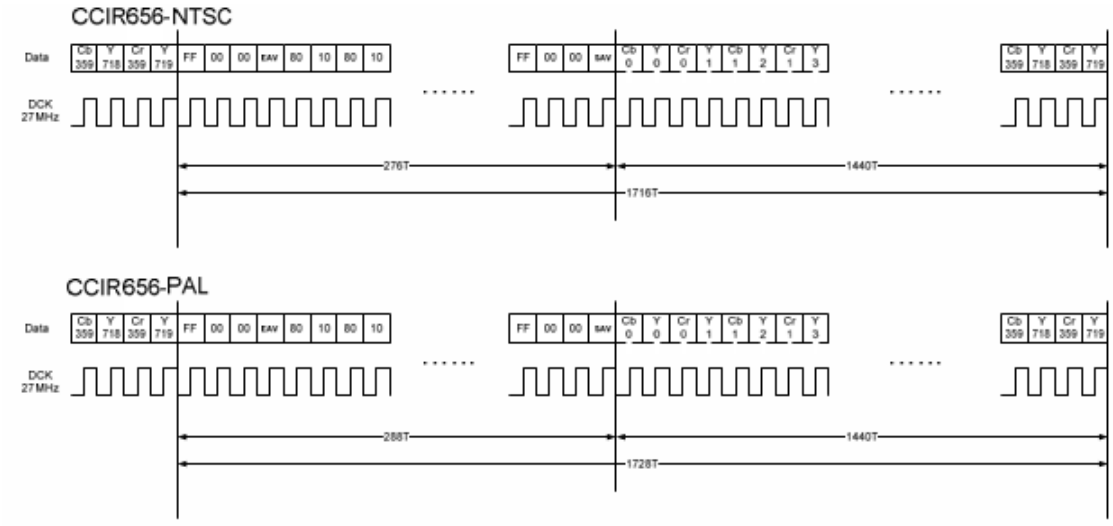


Figure : CCIR_656 Mode Data format

XY							
D7	D6	D5	D4	D3	D2	D1	D0
1	F	V	H	P3	P2	P1	P0

8.4.4 CCIR656/YUV640/YUV720 to RGB Conversion Formula

Rn = 1.164 x [(Y_{2n-1} + Y_{2n}) / 2 - 16] + 1.596 x (Cr_n-128)
Gn = 1.164 x [(Y_{2n-1} + Y_{2n}) / 2 - 16] - 0.813 x (Cr_n-128) – 0.392 x (Cb_n-128) Bn = 1.164 x [(Y_{2n-1} + Y_{2n}) / 2 - 16] + 2.017 x (Cb_n-128)

Where Y : 16~235 Cr : 16~240 Cb : 16~240

8.5 Input Timing Format

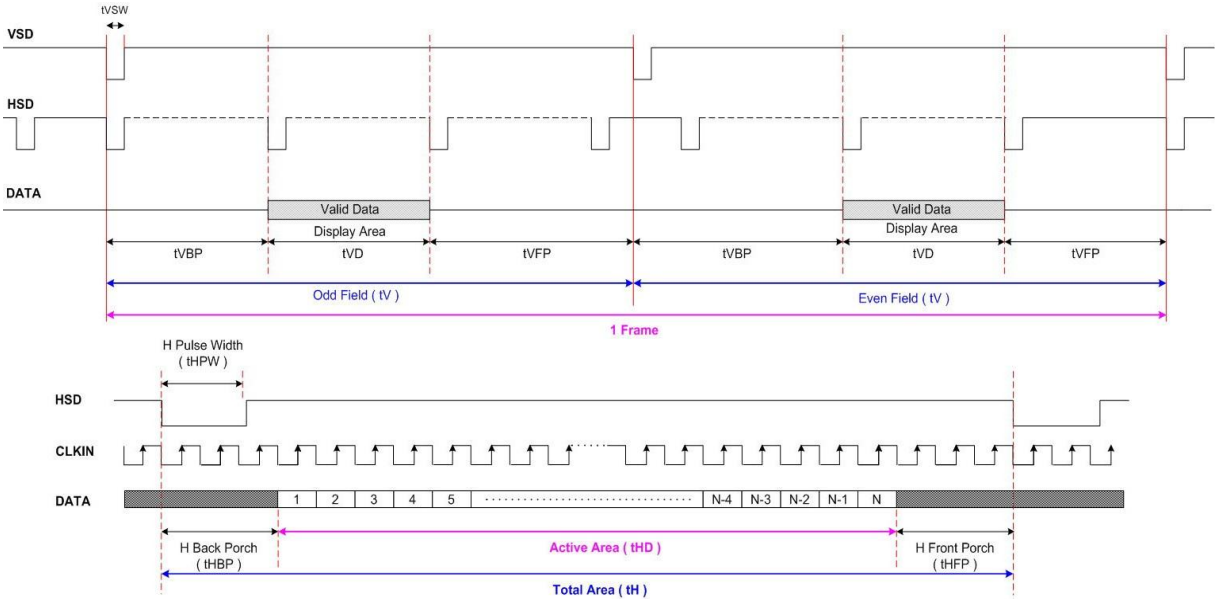


Figure : 8-bit RGB/8-bit Dummy RGB/YUV /Parallel RGB Input timing chart

8.5.1 8-bit RGB input timing

Parameter	Symbol	Interlace			Unit
		Min.	Typ.	Max.	
CLKIN frequency	fCLKIN	13.5	27	27.19	MHz
HSD period	tH	1024	1716	1728	CLKIN
HSD display period	tHD	960			CLKIN
HSD back porch	tHBP	50	70	255	CLKIN
HSD front porch	tHFP	14	686	718	CLKIN
HSD pulse width	tHPW	1	1	tHBP-1	CLKIN
VSD period time	tV	242.5	262.5	450.5	H

Vertical display area		tVD	240			H
VSD back porch	Odd field	tVBP	3	21	31	H
	Even field		3.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1 CLKIN	1CLKIN	6H	
1 Frame			485	525	901	H

Table： 8-bit RGB input timing

8.5.2 **8-bit Dummy RGB input timing**

8.5.2.1 8-bit Dummy RGB (320 mode/NTSC/24.535Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	20.45	24.535	30	MHz
HSD period		tH	1306	1560	1907	CLKIN
HSD display period		tHD	1280			CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	39	372	CLKIN
HSD pulse width		tHPW	1	1	200	CLKIN
VSD period time		tV	242.5	262.5	450.5	H
Vertical display area		tVD	240			H
VSD back porch	Odd field	tVBP	3	21	31	H
	Even field		3.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame			485	525	901	H

Table： 8-bit Dummy RGB (320 mode/NTSC/24.535Mhz) input timing

8-bit Dummy RGB (320 mode/PAL/24.375Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	20.45	24.375	30	MHz
HSD period		tH	1306	1560	1920	CLKIN
HSD display period		tHD	1280			CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	39	385	CLKIN
HSD pulse width		tHPW	1	1	200	CLKIN
VSD period time		tV	292.5	312.5	450.5	H
Vertical display area		tVD	288			H
VSD back porch	Odd field	tVBP	3	23	34	H
	Even field		3.5	23.5	34.5	
VSD front porch	Odd field	tVFP	1.5	1.5	128.5	H
	Even field		1	1	128	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame			585	625	901	H

Table： - 8 bit Dummy RGB (320 mode/PAL/24.375Mhz) input timing

8.5.2.2 8-bit Dummy RGB (360 mode/NTSC/27Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	23	27	30	MHz
HSD period		tH	1466	1716	1907	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	35	212	CLKIN
HSD pulse width		tHPW	1	1	200	CLKIN
VSD period time		tV	242.5	262.5	450.5	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	3	21	31	H
	Even field		3.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame			485	525	901	H

Table : 8-bit Dummy RGB (360 mode/NTSC/27Mhz) input timing

8.5.2.3 8-bit Dummy RGB (360 mode/PAL/27Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	23	27	30	MHz
HSD period		tH	1466	1728	1920	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	47	225	CLKIN
HSD pulse width		tHPW	1	1	200	CLKIN
VSD period time		tV	292.5	312.5	450.5	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	3	23	34	H
	Even field		3.5	23.5	34.5	
VSD front porch	Odd field	tVFP	1.5	1.5	128.5	H
	Even field		1	1	128	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame			585	625	901	H

Table : 8-bit Dummy RGB (360 mode/PAL/27Mhz) input timing

8.5.3 YUV720 and YUV640 input timing

8.5.3.1 YUV720 mode/NTSC input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	27	-	MHz
HSD period		tH	-	1716	-	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	36	-	CLKIN
HSD pulse width		tHPW	-	1	-	CLKIN
VSD period time		tV	-	262.5	-	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	-	21	-	H
	Even field		-	21.5	-	
VSD front porch	Odd field	tVFP	-	1.5	-	
	Even field		-	1	-	
VSD pulse width		tVSW	-	1	1	
1 Frame			-	525	-	

Table : YUV720 mode/NTSC input timing

8.5.3.2 YUV720 mode/PAL input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	27	-	MHz
HSD period		tH	-	1728	-	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	48	-	CLKIN
HSD pulse width		tHPW	-	1	-	CLKIN
VSD period time		tV	-	312.5	-	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	-	24	-	H
	Even field		-	24.5	-	
VSD front porch	Odd field	tVFP	-	0.5	-	H
	Even field		-	0	-	
VSD pulse width		tVSW	-	1	-	CLKIN
1 Frame			-	625	-	H

Table : YUV720 mode/PAL input timing

8.5.3.3 YUV640 mode/NTSC input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	24.535	-	MHz
SD period		tH	-	1560	-	CLKIN
HSD display period		tHD	1280			CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	40	-	CLKIN
HSD pulse width		tHPW	-	1	-	CLKIN
VSD period time		tV	-	262.5	-	H
Vertical display area		tVD	240			H
VSD back porch	Odd field	tVBP	-	21	-	H
	Even field		-	21.5	-	
VSD front porch	Odd field	tVFP	-	1.5	-	H
	Even field		-	1	-	
VSD pulse width		tVSW	-	1	-	CLKIN
1 Frame			-	525	-	H

Table : YUV640 mode/NTSC input timing

8.5.3.4 YUV640 mode/PAL input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	24.375	-	MHz
HSD period		tH	-	1560	-	CLKIN
HSD display period		tHD	1280			CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	40	-	CLKIN
HSD pulse width		tHPW	-	1	-	CLKIN
VSD period time		tV	-	312.5	-	H
Vertical display area		tVD	288			H
VSD back porch	Odd field	tVBP	-	24	-	H
	Even field		-	24.5	-	
VSD front porch	Odd field	tVFP	-	0.5	-	H
	Even field		-	0	-	
VSD pulse width		tVSW	-	1	-	CLKIN
1 Frame			-	625	-	H

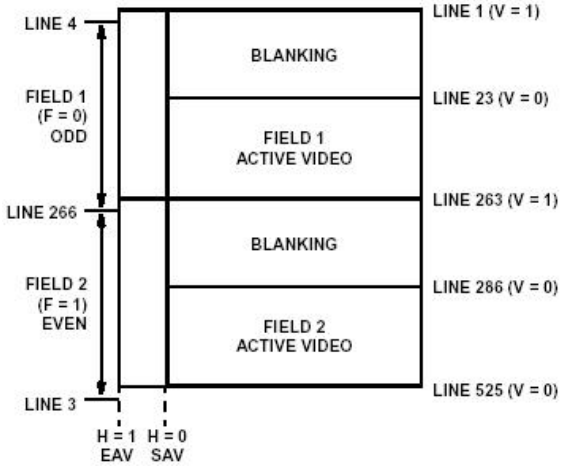
Table : YUV640 mode/PAL input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	6.14	-	MHz
HSD period		tH	-	390	-	CLKIN
HSD display period		tHD		320		CLKIN
HSD back porch		tHBP	40	61	-	CLKIN
HSD front porch		tHFP	-	9	-	CLKIN
HSD pulse width		tHPW	-	1	-	CLKIN
VSD period time		tV	-	262.5	-	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	-	21	-	H
	Even field		-	21.5	-	
VSD front porch	Odd field	tVFP	-	1.5	-	H
	Even field		-	1	-	
VSD pulse width		tVSW	-	1	-	CLKIN
1 Frame			-	525	-	H

Table : Parallel RGB input timing input timing

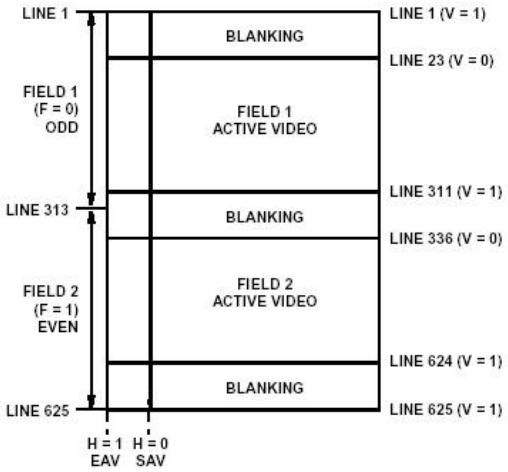
8.5.5 CCIR656 vertical input timing

8.5.5.1 NTSC mode



LINE NUMBER	F	V	H (EAV)	H (SAV)
1-3	1	1	1	0
4-22	0	1	1	0
23-262	0	0	1	0
263-265	0	1	1	0
266-285	1	1	1	0
286-525	1	0	1	0

8.5.5.2 PAL mode

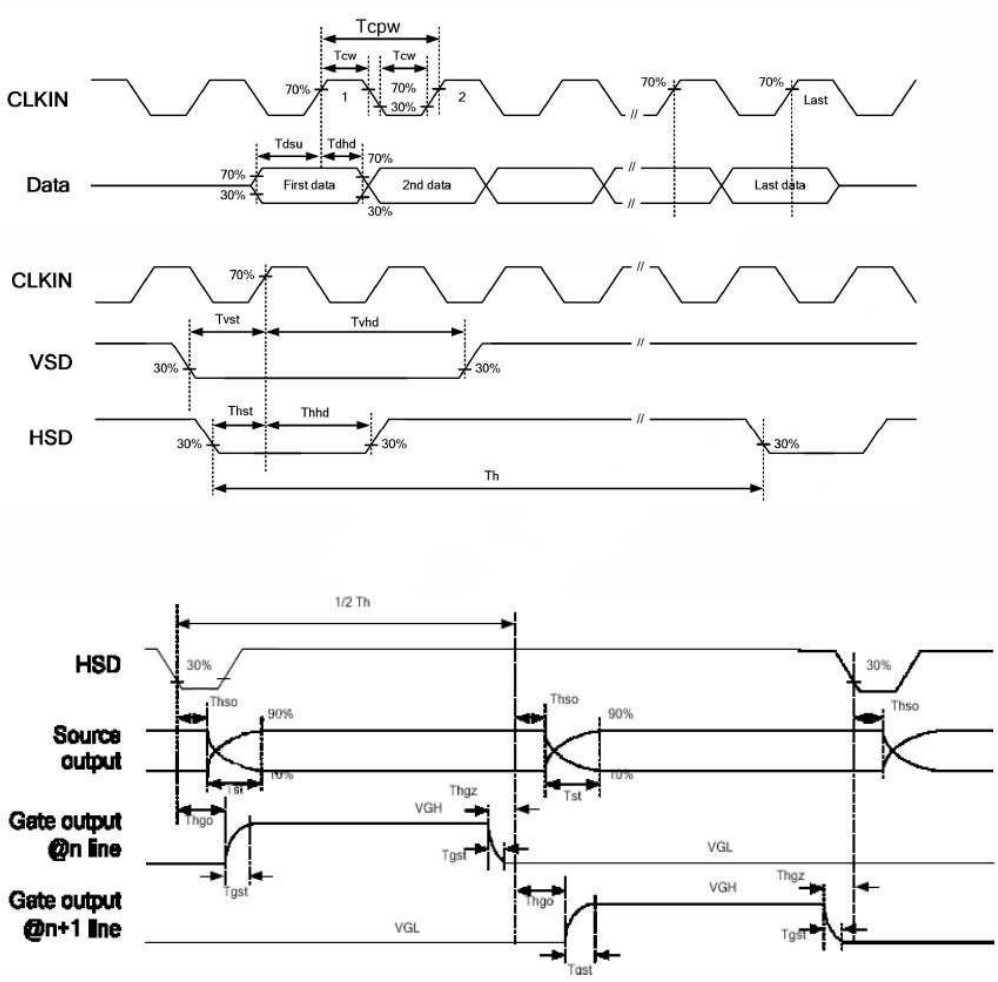


LINE NUMBER	F	V	H (EAV)	H (SAV)
1-22	0	1	1	0
23-310	0	0	1	0
311-312	0	1	1	0
313-335	1	1	1	0
336-623	1	0	1	0
624-625	1	1	1	0

	F	H	V
1	EVEN Field	EAV	BLANKING
0	Odd Field	SAV	ACTIVE VIDEO

9. AC Electrical Characteristics

9.1 AC Electrical Characteristics



(VDD=3.0~3.6V,VDDIO=AVDD=VDD,GND=AGND=0V, TA=25℃)

PARAMETER	Symbol	Spec.			Unit	Conditions
		Min.	Typ.	Max.		
HSD period time	Th	60	63.56	67	us	
HSD setup time	T_{hst}	12	-	-	ns	
HSD hold time	T_{hhd}	12	-	-	ns	
VSD setup time	T_{vst}	12	-	-	ns	
VSD hold time	T_{vhd}	12	-	-	ns	
Data setup time	T_{dsu}	12	-	-	ns	
Data hold time	T_{dhd}	12	-	-	ns	
Source output settling time	T_{ST}	-	-	8	us	R=5Kohm , C=30pF
Gate output settling time	Tgst	-	0.5	1	us	R=3Kohm , C=25pF
VCOM setting time	$T_{ST,}$vcom	-	-	9	us	R=200ohm , C=5nF

9.2 Power On/Off Sequence

9.2.1 Power on Sequence

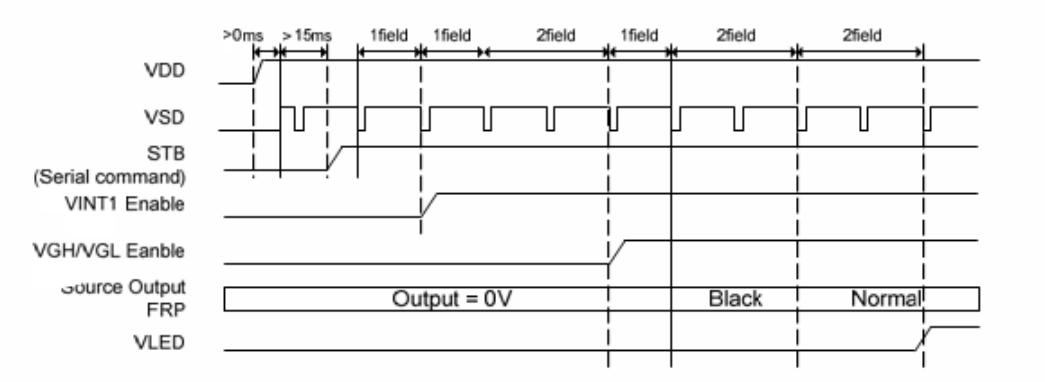


Figure : Power on sequence

9.2.2 Power off Sequence

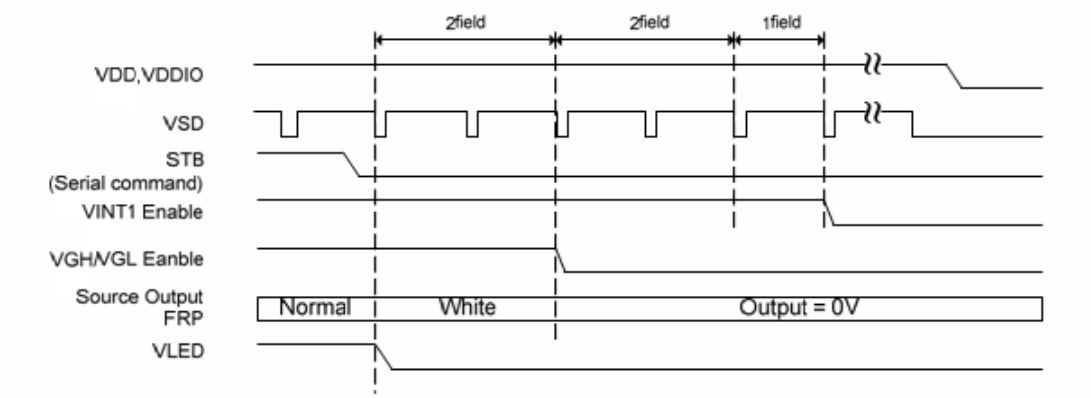


Figure : Power off sequence

10. Optical Specification

Ta=25℃

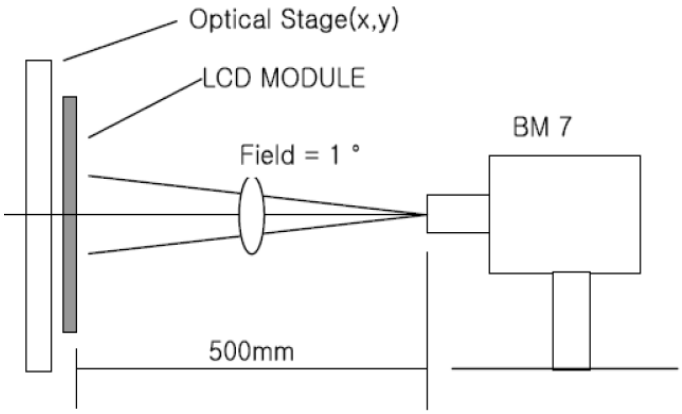
Item		Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio		CR	θ=0°	400	500	-		Note1 Note2
Response Time		Ton/ Toff	25℃	-	30	40	ms	Note1 Note3
View Angles		ΘT	CR≧10	50	60	-	Degree	Note 4
		ΘB		60	70	-		
		ΘL		60	70	-		
		θR		60	70	-		
Chromaticity	White	x	Brightness is on	0.260	0.310	0.360		Note5, Note1
		y		0.280	0.330	0.380		
	Red	x		0.518	0.568	0.618		
		y		0.287	0.337	0.387		
	Green	x		0.300	0.350	0.400		
		y		0.494	0.544	0.594		
	Blue	x		0.106	0.156	0.206		
		y		0.059	0.109	0.159		
NTSC		S			40		%	Note5
Luminance		L		200	250	-	cd/m^2	Note1 Note6
Uniformity		U		75	80	-	%	Note1 Note7

Test condition: VF=3.2V, IL=20mA(Backlight current), the ambient temperature is 25℃.

Note 1: Definition of optical measurement system.

Temperature = 25℃(±3℃)

LED back-light: ON, Environment brightness < 150 lx

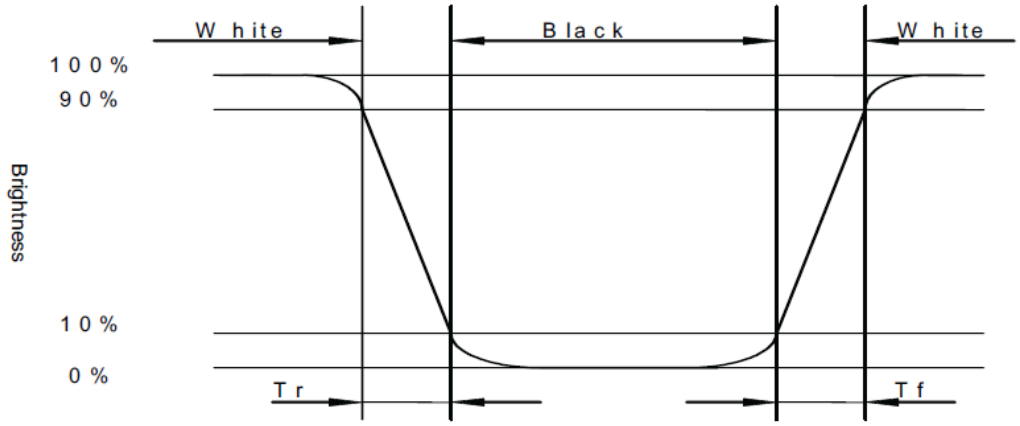


Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

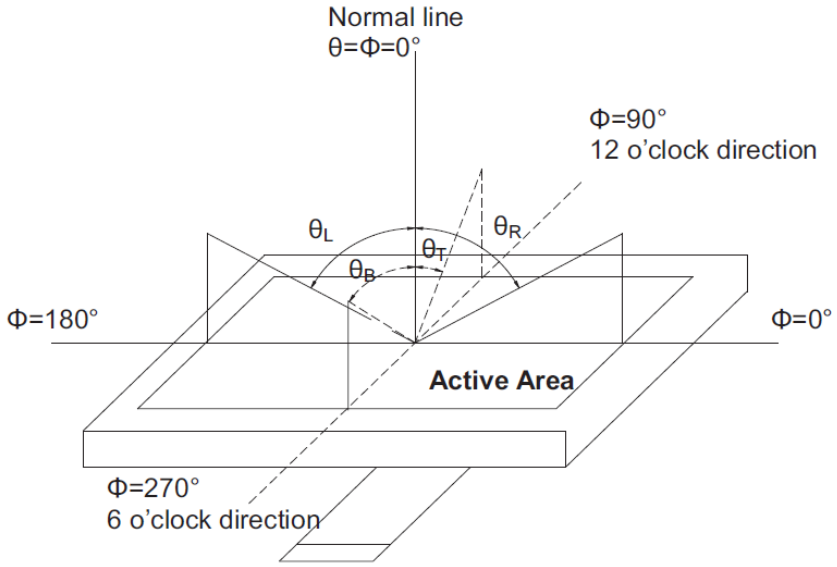
Note 3: Response time is defined as follow:

Response time is the time required for the display to transition from black to white (Rise Time, Tr) and from white to black(Decay Time, Tf).



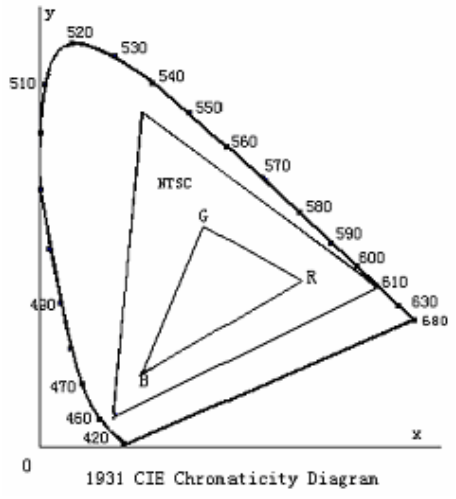
Note 4: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the LCD.



Note 5: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of LCD.



$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 6: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels "White" at the center of display area on optimum contrast.

Note 7: Luminance Uniformity is defined as follow:

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

$$\text{Uniformity(U)} = \frac{\text{Minimum Luminance(brightness) in 9 points}}{\text{Maximum Luminance(brightness) in 9 points}}$$

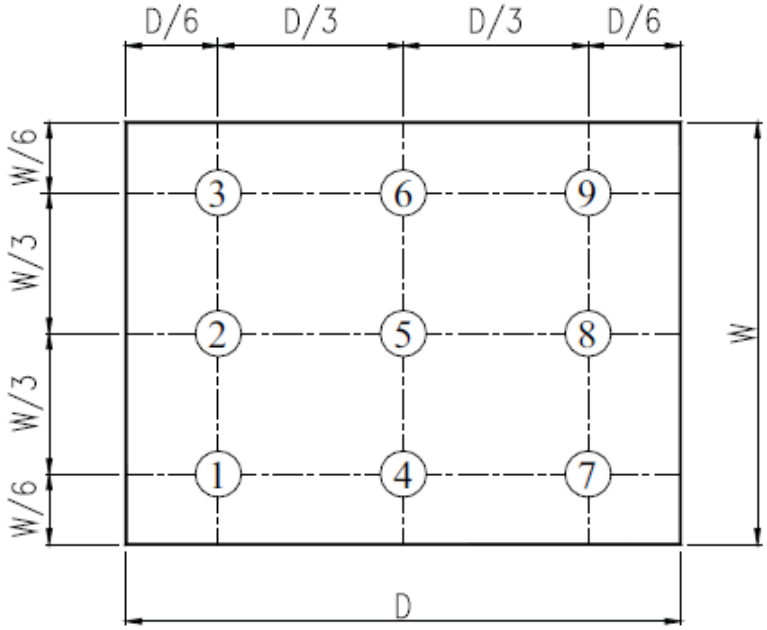


Fig. 2 Definition of uniformity

11. Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ts=+70℃, 120hrs	Per table in below
2	Low Temp Operation	Ta=-20℃, 120hrs	Per table in below
3	High Temp Storage	Ta=+80℃, 120hrs	Per table in below
4	Low Temp Storage	Ta=-30℃, 120hrs	Per table in below
5	High Temp & High Humidity Storage	Ta=+40℃, 90% RH 120 hours	Per table in below (polarizer discoloration is excluded)
6	Thermal Shock (Non-operation)	-30℃ 30 min~+70℃ 30 min, Change time:5min, 10 Cycles	Per table in below
7	ESD (Operation)	C=150pF, R=330Ω，5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times;	Per table in below
8	Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z.	Per table in below
9	Shock (Non-operation)	60G 6ms, ±X,±Y,±Z 3times, for each direction	Per table in below
10	Package Drop Test	Height:80 cm, 1 corner, 3 edges, 6 surfaces	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the LCD Panel
Alignment of LCD Panel	No Bubbles in the LCD Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

12. Precautions for Use of LCD Modules

12.1 Safety

The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

12.2 Handling

A. The LCD and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

12.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the LCD module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.

12.4Storage

A. Store the products in a dark place at +25℃±10℃ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

12.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

12.6 Cautions for installing and assembling

Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.