# DATA SHEET

# SBN1661G_M18, SBN1661G_M02, SBN0080G_S18, SBN0080G_S02

## Dot-matrix STN LCD Driver with 32-row x 80-column Display Data Memory

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# 1 GENERAL

## 1.1 Description

The SBN1661G_X is a series of STN LCD SEGMENT/COMMON drivers. The series has four members:

- the SBN1661G_M18,
- the SBN1661G_M02,
- the SBN0080G_S18, and
- the SBN0080G_S02.

Both the SBN1661G_M18 and the SBN1661G_M02 can drive 16 COMMONs and 61 SEGMENTs and can be used as master in a master-slave connection. They both have 32-row x 80-column Display Data Memory. Functionally, their only difference is that the SBN1661G_M18 has an on-chip RC-type oscillator and can provide clock to slave, while the SBN1661G_M02 does not have an on-chip oscillator and needs external clock source.

Both the SBN0080G_S18 and the SBN0080G_S02 are purely SEGMENT drivers. They do not have COMMON outputs and are used for segment expansion in a master-slave connection. Both devices need either a master or an external clock source to provide clock. The only difference between these two chips is their operating frequency. The SBN0080G_S18's operating frequency is 18 KHz, while the SBN0080G_S02's operating frequency is 2KHz.

All four devices have on-chip Display Data Memory of 32-rows x 80-columns, for storing display data. Dot-matrix mapping method is used to drive the LCD panel. Therefore, a bit of the Display Data Memory corresponds to a pixel on the LCD panel. SEGMENT drivers provide display data to the LCD panel and COMMON drivers provide row-scanning signal.

All four devices have a set of internal registers. These internal registers must be properly programmed to ensure proper operation of the devices.

Display on the LCD panel is controlled by a host microcontroller. All four devices communicate with the host microcontroller via data bus and control bus. The data bus is 8-bit wide. The control bus are READ, WRITE, and Chip Select. The host microcontroller can perform READ/WRITE operations to the internal registers and Display Data RAM of all four devices. A wide variety of microcontrollers can easily interface with the devices, as the devices can accept both 80-type interface timing and 68-type interface timing. The selection of interface timing is via the dual-function RESET/IF pin.

### 1.2 Features

- Four members of the SBN1661G_X series:
  - the SBN1661G_M18,
  - the SBN1661G_M02,
  - the SBN0080G_S18, and
  - the SBN0080G_S02
- 16 COMMON, 61 SEGMENT STN LCD driver (the SBN1661G_M18 and the SBN1661G_M02).
- 80 SEGMENT STN LCD driver for expanding segment number (the SBN0080G_S18 and the SBN0080G_S02).
- On-chip Display Data Memory: 32-row x 80-column (totally 2560 bits).
- Dot Matrix Mapping between the Display Data Memory bit and LCD pixel.
- A “0” stored in the Display Data Memory bit corresponds to an OFF-pixel on the LCD panel; a “1” stored in the Display Data Memory bit corresponds to an ON-pixel on the LCD panel.
- 5-level external LCD bias.
- Display duty cycle: 1/16, 1/32 for all four devices.
- Two types of interface timing with a host microcontroller: the 80-type microcontroller and the 68-type microcontroller.
- Dual function RESET/IF input for chip reset and selection of microcontroller interface timing.
- 8-bit parrallel data bus; READ, WRITE, CHIP SELECT control bus.
- A set of internal registers: Display ON/OFF, Display Start Line, Static Drive ON/OFF, Memory Page Address, Memory Column Address, Duty Selection, Memory Column/Segment mapping, and Status.
- Display Data Read/Write commands and Software Reset command.
- Read-Modify-Write command for block data transfer from the host microcontroller to the Display Data Memory.
- Power-saving mode.
- On-chip RC-type oscillator, requiring only an external resistor (the SBN1661G_M18).
- Operating voltage range ($V_{DD}$): 2.7 ~ 5.5 volts.
- LCD bias voltage ($V_{LCD}$=V5-$V_{DD}$): -13 volts (max.).
- Operating frequency range: 2 KHz, 18 KHz.
- Operating temperature range: -20 to +75 °C.
- Storage temperature range: -55 to +125 °C.

### 1.3 Ordering information

**Table 1** Product types

| Product Name | Clock frequency | | Number of segment driver | Number of common driver | duty cycle |
|---|---|---|---|---|---|
| | on-chip | External | | | |
| SBN1661G_M18 | 18 KHz | 18 KHz | 61 | 16 | 1/16, 1/32 |
| SBN1661G_M02 | | 2 KHz | | | |
| SBN0080G_S18 | | 18 KHz | 80 | 0 | |
| SBN0080G_S02 | | 2 KHz | | | |

**Table 2** Ordering information

| PRODUCT TYPE | DESCRIPTION |
|---|---|
| SBN1661G_M18-LQFPG | LQFP100 Pb-free package. |
| SBN1661G_M18-QFPG | QFP100 Pb-free package. |
| SBN1661G_M18-LQFP | LQFP100 general package. |
| SBN1661G_M18-QFP | QFP100 general package. |
| SBN1661G_M18-D | tested die. |
| SBN1661G_M02-LQFPG | LQFP100 Pb-free package. |
| SBN1661G_M02-QFPG | QFP100 Pb-free package. |
| SBN1661G_M02-LQFP | LQFP100 general package. |
| SBN1661G_M02-QFP | QFP100 general package. |
| SBN1661G_M02-D | tested die. |
| SBN0080G_S18-LQFPG | LQFP100 Pb-free package. |
| SBN0080G_S18-QFPG | QFP100 Pb-free package. |
| SBN0080G_S18-LQFP | LQFP100 general package. |
| SBN0080G_S18-QFP | QFP100 general package. |
| SBN0080G_S18-D | tested die. |
| SBN0080G_S02-LQFPG | LQFP100 Pb-free package. |
| SBN0080G_S02-QFPG | QFP100 Pb-free package. |
| SBN0080G_S02-LQFP | LQFP100 general package. |
| SBN0080G_S02-QFP | QFP100 general package. |
| SBN0080G_S02-D | tested die. |

## 2 FUNCTIONAL BLOCK DIAGRAM AND DESCRIPTION

### 2.1 Funtional block diagram (SBN1661G_M18, SBN1661G_M02)

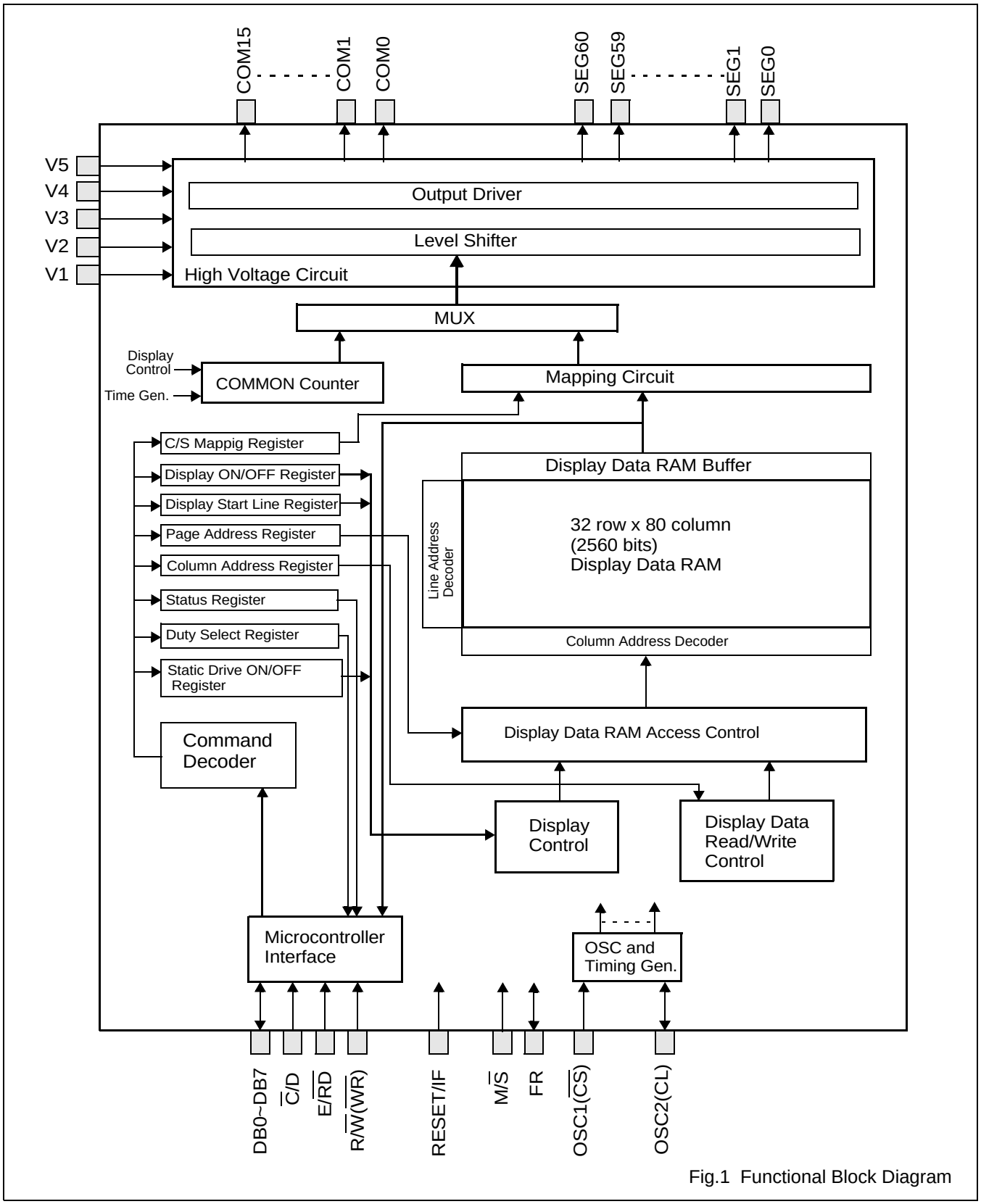
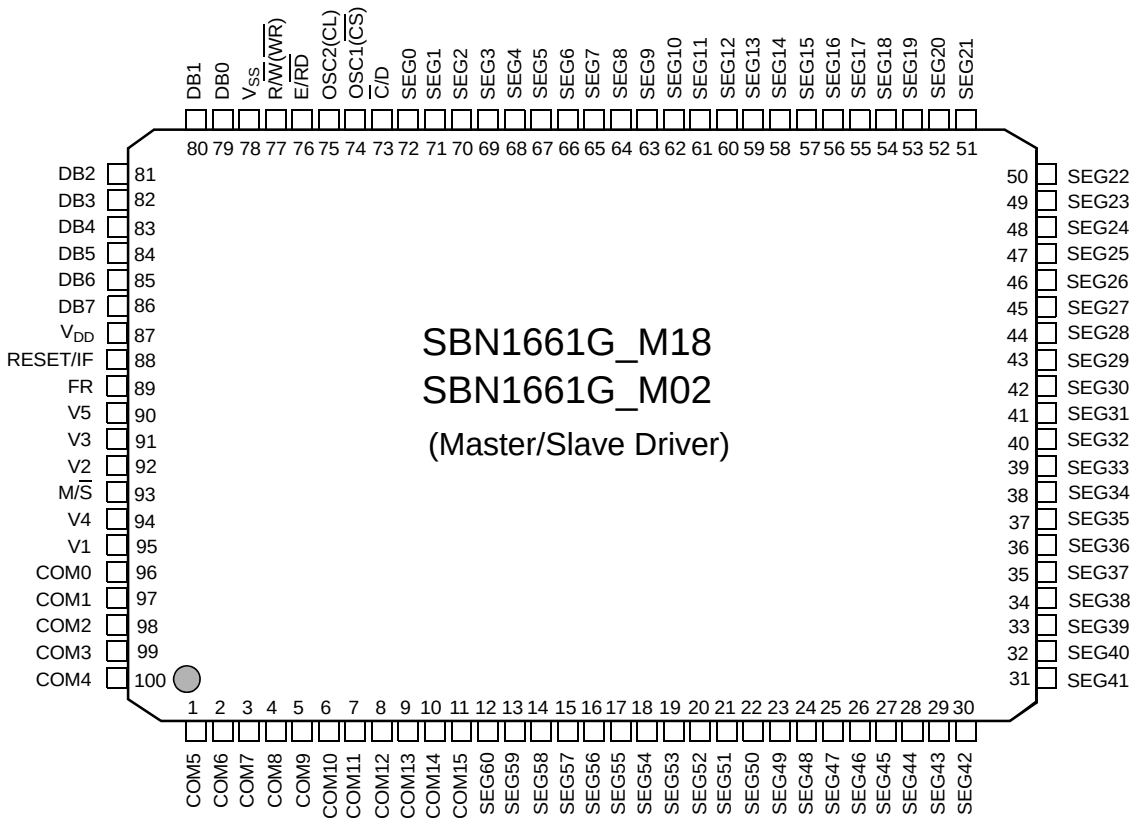



Fig.1 Functional Block Diagram

## 3 PIN(PAD) ASSIGNMENT, PAD COORDINATES, SIGNAL DESCRIPTION

### 3.1 The SBN1661G_M18 and SBN1661G_M02 pinning diagram (LQFP100)




Note:

(1) For the SBN1661G_M18, pin 74 is OSC1 and pin 75 is OSC2.

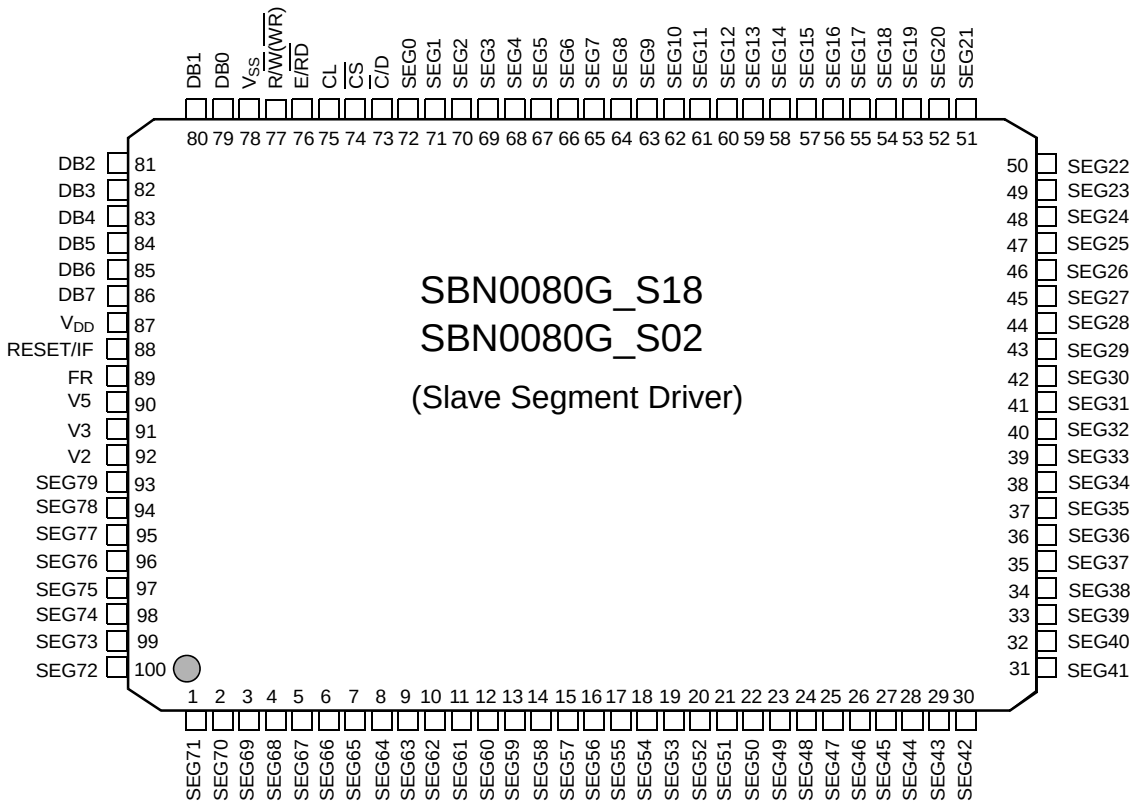
(2) For the SBN1661G_M02, pin 74 is $\overline{CS}$ and pin 75 is CL.

(3) All other pins of both devices have the same pin(pad) assignment.

(4) Both devices can be used as master or slave, by setting their M/$\overline{S}$ pin.

Fig.2 The SBN1661G_M18 , the SBN1661G_M02 pin assignment of LQFP100 package.

### 3.2 The SBN0080G_S18, the SBN0080G_S02 pinning diagram (LQFP100)



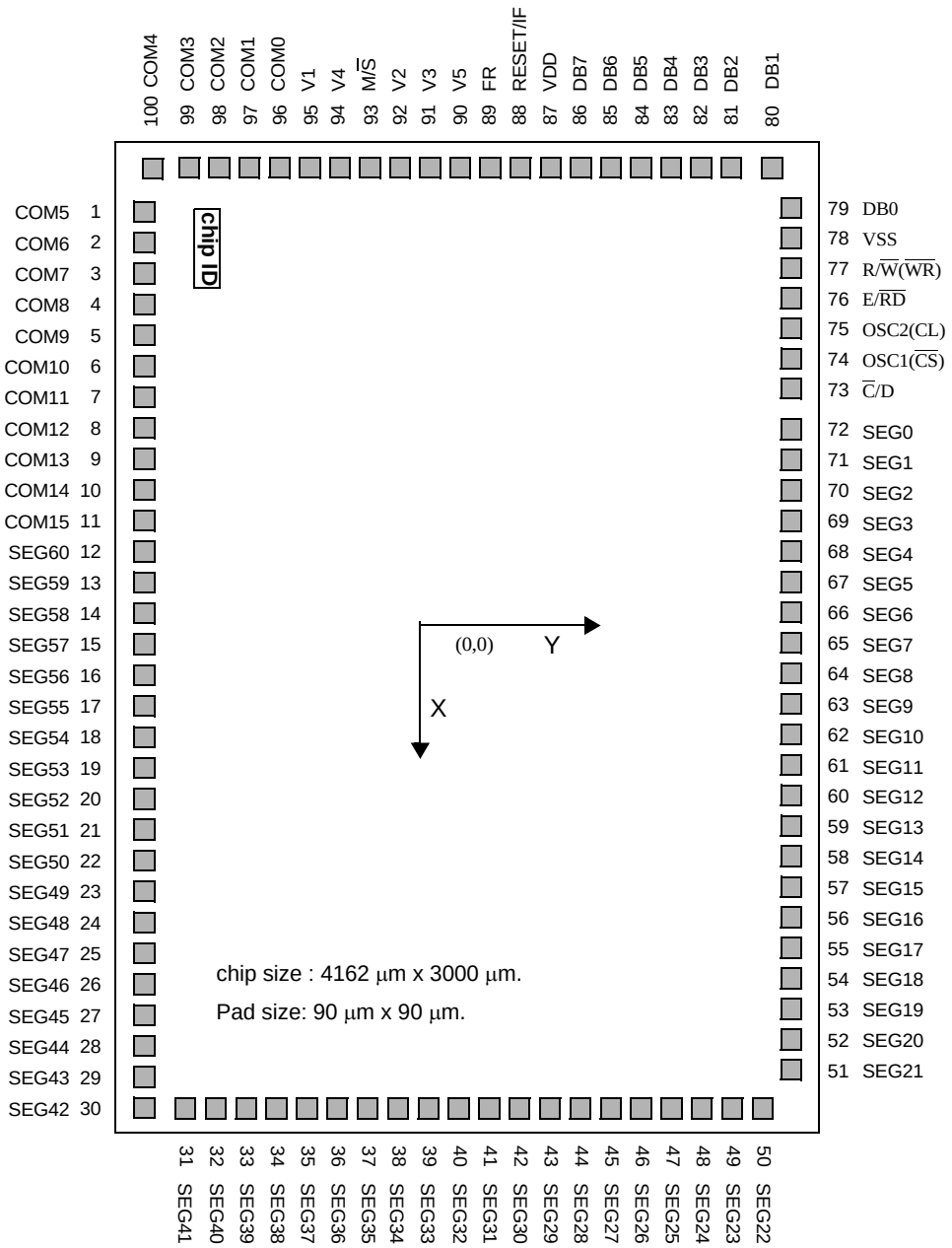

Note:

(1) Both devices have the same pin(pad) assignment.

(2) Both devices can be used only as Slave Segment Driver.

Fig.3 The SBN0080G_S18, the SBN0080G_S02 pin assignment of LQFP100 package.

### 3.3 The SBN1661G_M18 , SBN1661G_M02 pad placement




Note:

(1) The SBN1661G_M18 and the SBN1661G_M02 have the same pad placement.

(2) The chip ID of the SBN1661G_M18 is AT18001-01.

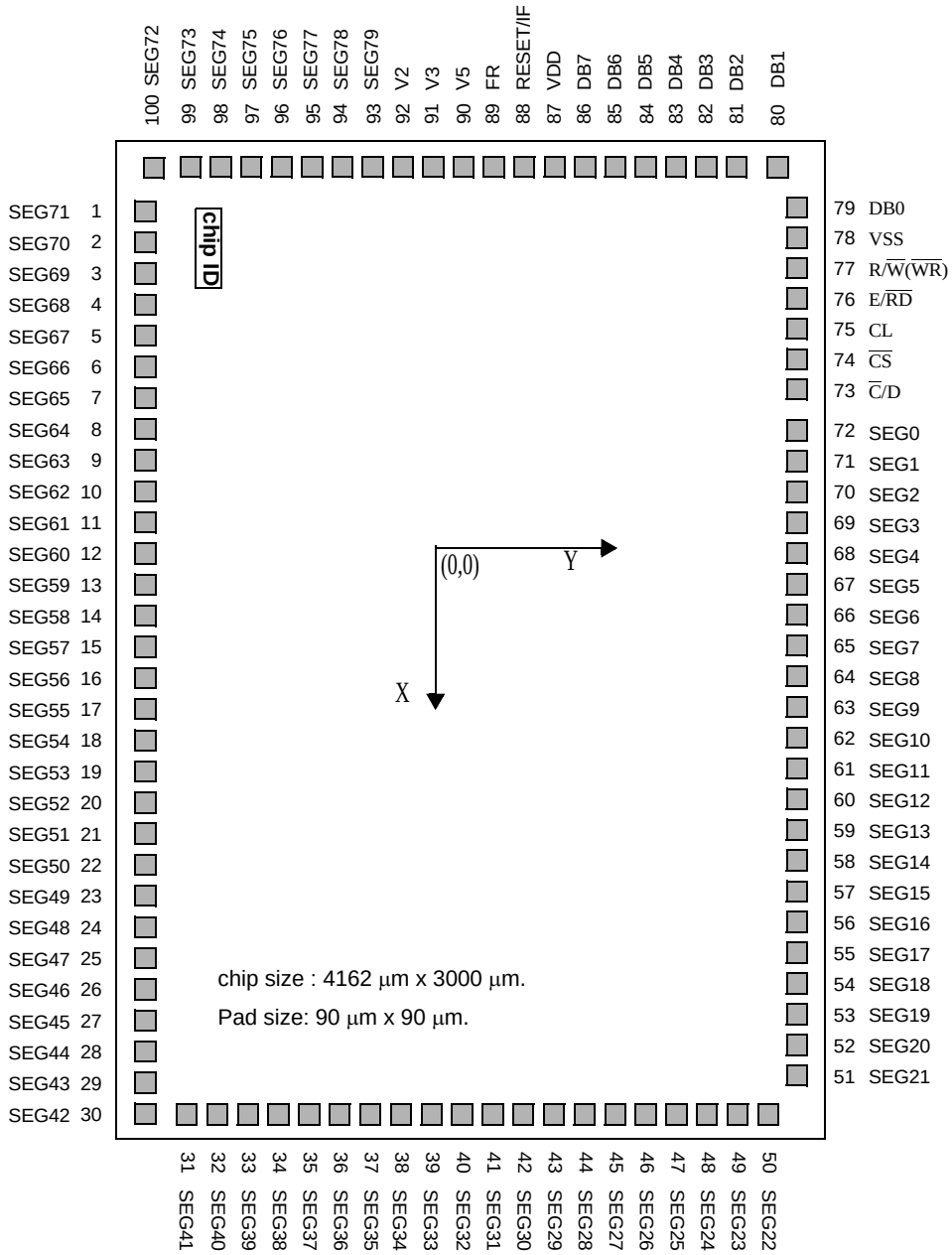
(3) The chip ID of the SBN1661G_M02 is AT18001-02.

(4) The die origin is at the center of the chip.

(5) For chip_on_board_bonding, **chip carrier** should be connected to VDD or left open. Chip carrier is the metal pad to which the die is attached.

Fig.4 The SBN1661G_M18, SBN1661G_M02 pad placement

### 3.4 The SBN0080G_S18 , SBN0080G_S02 pad placement




Note:

(1) The SBN0080G_S18 and the SBN0080G_S02 have the same pad placement.

(2) The chip ID of the SBN0080G_S18 is AT18001-03

(3) The chip ID of the SBN0080G_S02 is AT18001-04.

(4) The die origin is at the center of the chip.

(5) For chip_on_board_bonding, **chip carrier** should be connected to VDD or left open. Chip carrier is the metal pad to which the die is attached.

Fig.5 The SBN0080G_S18, SBN0080G_S02 pad placement

### 3.5 The SBN1661G_M18, SBN1661G_M02 pad coordinates

**Table 3** The SBN1661G_M18, SBN1661G_M02 pad coordinates (unit: μm)

| PAD NO. | PAD NAME | X | Y |
|---|---|---|---|
| 1 | COM5 | -1824 | -1430 |
| 2 | COM6 | -1694 | -1430 |
| 3 | COM7 | -1569 | -1430 |
| 4 | COM8 | -1444 | -1430 |
| 5 | COM9 | -1319 | -1430 |
| 6 | COM10 | -1186 | -1430 |
| 7 | COM11 | -1053 | -1430 |
| 8 | COM12 | -920 | -1430 |
| 9 | COM13 | -787 | -1430 |
| 10 | COM14 | -654 | -1430 |
| 11 | COM15 | -521 | -1430 |
| 12 | SEG60 | -388 | -1430 |
| 13 | SEG59 | -255 | -1430 |
| 14 | SEG58 | -122 | -1430 |
| 15 | SEG57 | 11 | -1430 |
| 16 | SEG56 | 144 | -1430 |
| 17 | SEG55 | 277 | -1430 |
| 18 | SEG54 | 410 | -1430 |
| 19 | SEG53 | 543 | -1430 |
| 20 | SEG52 | 676 | -1430 |
| 21 | SEG51 | 809 | -1430 |
| 22 | SEG50 | 942 | -1430 |
| 23 | SEG49 | 1075 | -1430 |
| 24 | SEG48 | 1208 | -1430 |
| 25 | SEG47 | 1341 | -1430 |
| 26 | SEG46 | 1474 | -1430 |
| 27 | SEG45 | 1607 | -1430 |
| 28 | SEG44 | 1740 | -1430 |
| 29 | SEG43 | 1873 | -1430 |
| 30 | SEG42 | 2006 | -1430 |
| 31 | SEG41 | 2011 | -1272 |
| 32 | SEG40 | 2011 | -1137 |
| 33 | SEG39 | 2011 | -1002 |
| 34 | SEG38 | 2011 | -867 |
| 35 | SEG37 | 2011 | -732 |
| 36 | SEG36 | 2011 | -597 |
| 37 | SEG35 | 2011 | -462 |
| 38 | SEG34 | 2011 | -327 |
| 39 | SEG33 | 2011 | -192 |
| 40 | SEG32 | 2011 | -57 |
| 41 | SEG31 | 2011 | 78 |
| 42 | SEG30 | 2011 | 213 |
| 43 | SEG29 | 2011 | 348 |
| 44 | SEG28 | 2011 | 483 |
| 45 | SEG27 | 2011 | 618 |
| 46 | SEG26 | 2011 | 753 |
| 47 | SEG25 | 2011 | 883 |
| 48 | SEG24 | 2011 | 1013 |
| 49 | SEG23 | 2011 | 1143 |
| 50 | SEG22 | 2011 | 1273 |
| 51 | SEG21 | 1842 | 1430 |
| 52 | SEG20 | 1712 | 1430 |
| 53 | SEG19 | 1582 | 1430 |
| 54 | SEG18 | 1452 | 1430 |
| 55 | SEG17 | 1322 | 1430 |
| 56 | SEG16 | 1192 | 1430 |
| 57 | SEG15 | 1062 | 1430 |
| 58 | SEG14 | 932 | 1430 |
| 59 | SEG13 | 802 | 1430 |
| 60 | SEG12 | 672 | 1430 |
| 61 | SEG11 | 542 | 1430 |
| 62 | SEG10 | 412 | 1430 |
| 63 | SEG9 | 282 | 1430 |
| 64 | SEG8 | 152 | 1430 |
| 65 | SEG7 | 22 | 1430 |
| 66 | SEG6 | -108 | 1430 |
| 67 | SEG5 | -238 | 1430 |
| 68 | SEG4 | -368 | 1430 |
| 69 | SEG3 | -498 | 1430 |
| 70 | SEG2 | -628 | 1430 |
| 71 | SEG1 | -758 | 1430 |
| 72 | SEG0 | -888 | 1430 |
| 73 | $\overline{C}$/D | -1062 | 1430 |
| 74 | OSC1 | -1194 | 1430 |
| 75 | OSC2 | -1326 | 1430 |
| 76 | E/$\overline{RD}$ | -1458 | 1430 |
| 77 | R/$\overline{W}$($\overline{WR}$) | -1590 | 1430 |
| 78 | VSS | -1722 | 1430 |
| 79 | DB0 | -1854 | 1430 |
| 80 | DB1 | -2011 | 1358 |
| 81 | DB2 | -2011 | 1176 |
| 82 | DB3 | -2011 | 1044 |
| 83 | DB4 | -2011 | 909 |
| 84 | DB5 | -2011 | 771 |
| 85 | DB6 | -2011 | 635 |
| 86 | DB7 | -2011 | 497 |
| 87 | VDD | -2011 | 358 |
| 88 | RESET/IF | -2011 | 212 |
| 89 | FR | -2011 | 81 |
| 90 | V5 | -2011 | -50 |
| 91 | V3 | -2011 | -180 |
| 92 | V2 | -2011 | -326 |
| 93 | M/$\overline{S}$ | -2011 | -456 |
| 94 | V4 | -2011 | -586 |
| 95 | V1 | -2011 | -716 |
| 96 | COM0 | -2011 | -846 |
| 97 | COM1 | -2011 | -976 |
| 98 | COM2 | -2011 | -1106 |
| 99 | COM3 | -2011 | -1236 |
| 100 | COM4 | -2011 | -1388 |

### 3.6 The SBN0080G_S18, SBN0080G_S02 pad coordinates

**Table 4** The SBN0080G_S18, SBN0080G_S02 pad coordinates ( unit: μm )

| Pad No. | Pad Name | X | Y |
|---|---|---|---|
| 1 | SEG71 | -1824 | -1430 |
| 2 | SEG70 | -1694 | -1430 |
| 3 | SEG69 | -1569 | -1430 |
| 4 | SEG68 | -1444 | -1430 |
| 5 | SEG67 | -1319 | -1430 |
| 6 | SEG66 | -1186 | -1430 |
| 7 | SEG65 | -1053 | -1430 |
| 8 | SEG64 | -920 | -1430 |
| 9 | SEG63 | -787 | -1430 |
| 10 | SEG62 | -654 | -1430 |
| 11 | SEG61 | -521 | -1430 |
| 12 | SEG60 | -388 | -1430 |
| 13 | SEG59 | -255 | -1430 |
| 14 | SEG58 | -122 | -1430 |
| 15 | SEG57 | 11 | -1430 |
| 16 | SEG56 | 144 | -1430 |
| 17 | SEG55 | 277 | -1430 |
| 18 | SEG54 | 410 | -1430 |
| 19 | SEG53 | 543 | -1430 |
| 20 | SEG52 | 676 | -1430 |
| 21 | SEG51 | 809 | -1430 |
| 22 | SEG50 | 942 | -1430 |
| 23 | SEG49 | 1075 | -1430 |
| 24 | SEG48 | 1208 | -1430 |
| 25 | SEG47 | 1341 | -1430 |
| 26 | SEG46 | 1474 | -1430 |
| 27 | SEG45 | 1607 | -1430 |
| 28 | SEG44 | 1740 | -1430 |
| 29 | SEG43 | 1873 | -1430 |
| 30 | SEG42 | 2006 | -1430 |
| 31 | SEG41 | 2011 | -1272 |
| 32 | SEG40 | 2011 | -1137 |
| 33 | SEG39 | 2011 | -1002 |
| 34 | SEG38 | 2011 | -867 |
| 35 | SEG37 | 2011 | -732 |
| 36 | SEG36 | 2011 | -597 |
| 37 | SEG35 | 2011 | -462 |
| 38 | SEG34 | 2011 | -327 |
| 39 | SEG33 | 2011 | -192 |
| 40 | SEG32 | 2011 | -57 |
| 41 | SEG31 | 2011 | 78 |
| 42 | SEG30 | 2011 | 213 |
| 43 | SEG29 | 2011 | 348 |
| 44 | SEG28 | 2011 | 483 |
| 45 | SEG27 | 2011 | 618 |
| 46 | SEG26 | 2011 | 753 |
| 47 | SEG25 | 2011 | 883 |
| 48 | SEG24 | 2011 | 1013 |
| 49 | SEG23 | 2011 | 1143 |
| 50 | SEG22 | 2011 | 1273 |
| 51 | SEG21 | 1842 | 1430 |
| 52 | SEG20 | 1712 | 1430 |
| 53 | SEG19 | 1582 | 1430 |
| 54 | SEG18 | 1452 | 1430 |
| 55 | SEG17 | 1322 | 1430 |
| 56 | SEG16 | 1192 | 1430 |
| 57 | SEG15 | 1062 | 1430 |
| 58 | SEG14 | 932 | 1430 |
| 59 | SEG13 | 802 | 1430 |
| 60 | SEG12 | 672 | 1430 |
| 61 | SEG11 | 542 | 1430 |
| 62 | SEG10 | 412 | 1430 |
| 63 | SEG9 | 282 | 1430 |
| 64 | SEG8 | 152 | 1430 |
| 65 | SEG7 | 22 | 1430 |
| 66 | SEG6 | -108 | 1430 |
| 67 | SEG5 | -238 | 1430 |
| 68 | SEG4 | -368 | 1430 |
| 69 | SEG3 | -498 | 1430 |
| 70 | SEG2 | -628 | 1430 |
| 71 | SEG1 | -758 | 1430 |
| 72 | SEG0 | -888 | 1430 |
| 73 | $\overline{C}$/D | -1062 | 1430 |
| 74 | $\overline{CS}$ | -1194 | 1430 |
| 75 | CL | -1326 | 1430 |
| 76 | E/$\overline{RD}$ | -1458 | 1430 |
| 77 | R/$\overline{W}$($\overline{WR}$) | -1590 | 1430 |
| 78 | VSS | -1722 | 1430 |
| 79 | DB0 | -1854 | 1430 |
| 80 | DB1 | -2011 | 1358 |
| 81 | DB2 | -2011 | 1176 |
| 82 | DB3 | -2011 | 1044 |
| 83 | DB4 | -2011 | 909 |
| 84 | DB5 | -2011 | 771 |
| 85 | DB6 | -2011 | 635 |
| 86 | DB7 | -2011 | 497 |
| 87 | VDD | -2011 | 358 |
| 88 | RESET/IF | -2011 | 212 |
| 89 | FR | -2011 | 81 |
| 90 | V5 | -2011 | -50 |
| 91 | V3 | -2011 | -180 |
| 92 | V2 | -2011 | -326 |
| 93 | SEG79 | -2011 | -456 |
| 94 | SEG78 | -2011 | -586 |
| 95 | SEG77 | -2011 | -716 |
| 96 | SEG76 | -2011 | -846 |
| 97 | SEG75 | -2011 | -976 |
| 98 | SEG74 | -2011 | -1106 |
| 99 | SEG73 | -2011 | -1236 |
| 100 | SEG72 | -2011 | -1388 |

### 3.7 Pin(pad) signal difference among the four members of the SBN1661G_X

All four members of the SBN1661G_X series have the same pad sequence and placement. However, some pins(pads) have different signals for different types. A comparison is given in Table 5.

**Table 5** Comparison of pin(pad) signals

| **Type** | **Pin(pad) 1~11** | **Pin(pad) 74** | **Pin(pad) 75** | **Pin(pad) 93** | **Pin(pad) 94** | **Pin(pad) 95** | **Pin(pad) 96~100** |
|---|---|---|---|---|---|---|---|
| SBN1661G_M18 | COM5~15 | OSC1 | OSC2 | M/$\overline{S}$ | V4 | V1 | COM0~4 |
| SBN1661G_M02 | COM5~15 | $\overline{CS}$ | CL | M/$\overline{S}$ | V4 | V1 | COM0~4 |
| SBN0080G_S18 | SEG71~61 | $\overline{CS}$ | CL | SEG79 | SEG78 | SEG77 | SEG76~72 |
| SBN0080G_S02 | | | | | | | |

### 3.8 Pin (pad) states after hardware RESET

**Table 6** Pin(pad) states after RESET

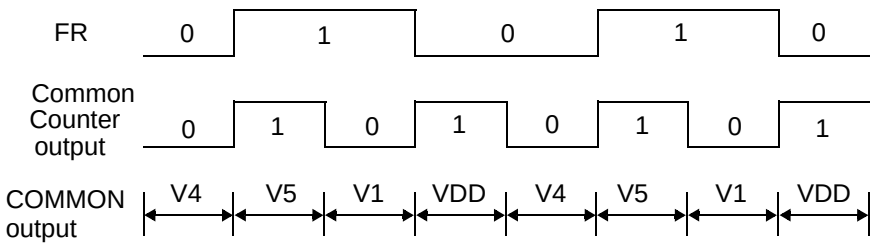
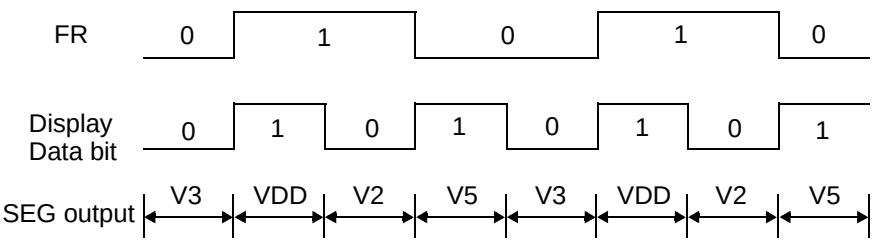
| | |
|---|---|
| **SBN1661G_M18, SBN1661G_M02** | |
| **signal** | **states after RESET** |
| DB0~DB7 | tri-state |
| COM0~COM15 | $V_{DD}$ |
| SEG0~SEG61 | $V_{DD}$ |
| FR(SBN1661G_M18) | tri-state |
| OSC2 (SBN1661G_M18) | tri-state |

| | |
|---|---|
| **SBN0080G_S18, SBN0080G_S02** | |
| **signal** | **states after RESET** |
| DB0~DB7 | tri-state |
| | |
| SEG0~SEG79 | $V_{DD}$ |
| | |
| | |

### 3.9 The SBN1661G_M18 and the SBN1661G_M02 signal description

**Table 7** Pin (pad) signal description

To avoid a latch-up effect at power-on: $V_{SS}$ – 0.5 V < voltage at any pin at any time < $V_{DD}$ + 0.5 V .

| Pin number | SYMBOL | I/O | DESCRIPTION |
|---|---|---|---|
| 1~11, 96~100 | COM5~15, COM0~4 | Output | COMMON driver outputs.<br>The output voltage level of COMMON outputs are decided by the combination of the alternating frame signal (FR) and the internal COMMON COUNTER, which generates raster-scanning COMMON signals. Depending on the value of the frame signal and the COMMON counter output, a single voltage level is selected from VDD, V1, V4, or V5 for COMMON driver , as shown in Fig. 6.<br>  <br>Fig.6 COMMON driver output voltage level |
| 12~72 | SEG60~0 | Output | SEGNENT driver outputs.<br>The output voltage level of SEGMENT outputs are decided by the combination of the alternating frame signal (FR) and display data. Depending on the value of the frame signal and the display data, a sinlge voltage level is selected from VDD, V2, V3, or V5 for SEGMENT driver, as shown in Fig. 7.<br>  <br>Fig.7 SEGMENT driver output voltage level |
| 73 | $\overline{C}$/D | Input | Selection of command or data.<br>When $\overline{C}$/D=0, the data on the 8-bit data bus (DB0~DB7) are either COMMAMD, data to be written to an internal register, or data read from the internal Status Register.<br>When $\overline{C}$/D=1, the data on the 8-bit data bus (DB0~DB7) are related to the Display Data Memory. They are the data to be written to or read from the Display Data Memory. |

| Pin number | SYMBOL | I/O | DESCRIPTION |
|---|---|---|---|
| 74 | OSC1 | Input | For the SBN1661G_M18, pin 74 is the OSC1 pin of the on-chip RC oscillator. It is the input pin to the oscillator. An external resistor should be connected across the OSC1 and the OSC2. |
| | $\overline{CS}$ | | For the SBN1661G_M02, pin 74 is the CS pin. Usually, a signal decoded from the host microcontroller address lines or a port line (C51) is connected to this pin. |
| 75 | OSC2 | Output | For the SBN1661G_M18, pin 75 is the OSC2 pin. It is the output pin of the on-chip RC oscillator. |
| | CL | Input | For the SBN1661G_M02, pin 75 is the CL pin. Clock from master or an external clock source should be added to this pin. |
| 76 | E/($\overline{RD}$) | Input | Enable signal (E) for the 68-type microcontroller, or READ ($\overline{RD}$) signal for the 80-type microcontroller.<br>If a 68-type microcotroller is selected as the host microcontroller, this pin should be connected to the ENABLE output of the microcontroller. A HIGH level on this pin indicates that the microcontroller intends to select the SBN1661G_X series.<br>If a 80-type microcontroller is selected as the host microcontroller, this pin should be connected to the $\overline{RD}$ output of the microcontroller. A LOW level on this pin indicates that the microcontroller intends to read from the SBN1661G_X series.. |
| 77 | R/$\overline{W}$($\overline{WR}$) | Input | Read/Write (R/$\overline{W}$) signal for the 68-type microcontroller, or WRITE($\overline{WR}$) signal for the 80-type microcontroller.<br>If a 68-type microcotroller is selected as the host microcontroller, this pin should be connected to the R/$\overline{W}$ output of the microcontroller. A HIGH level on this pin indicates that the microcontroller intends to read from the SBN1661G_X series. A LOW level on this pin indicates that the microcontroller intends to write to the SBN1661G_X series.<br>If a 80-type microcontroller is selected as the host microcontroller, this pin should be connected to the $\overline{WR}$ output of the microcontroller. A LOW level on this pin indicates that the microcontroller intends to write to the SBN1661G_X series. |
| 78 | $V_{SS}$ | | Ground pin. |
| 79~86 | DB0~DB7 | I/O | Bi-direction, tri-state 8-bit parallel data bus for interface with a host microcontroller.<br>This data bus is for data transfer between the host microcontroller and the SBN1661G_X. |
| 87 | $V_{DD}$ | Input | Power supply for logic part of the chip.<br>The $V_{DD}$ should be in the range from 2.7 volts to 5.5 volts. |

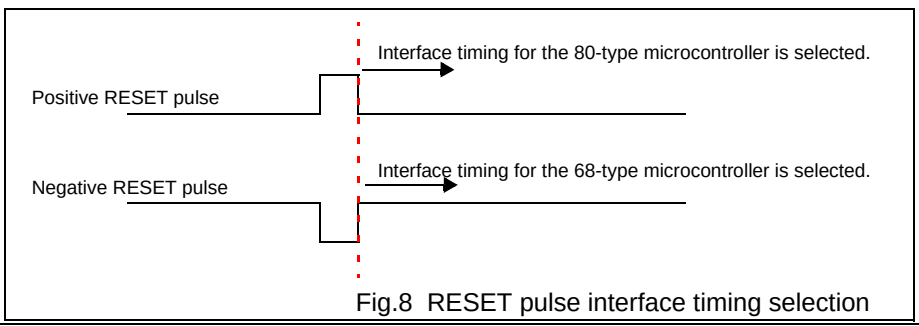
<table>
<tr><th>Pin number</th><th>SYMBOL</th><th>I/O</th><th>DESCRIPTION</th></tr>
<tr><td>88</td><td>RESET/IF</td><td>Input</td><td>Hardware RESET and interface type selection.<br><br>This pin is a dual function pin. It can be used to reset the SBN1661G_X and select the type of interface timing.<br><br>The hardware RESET is edge-sensitive. It is not level-sensitive. That is, either a falling edge or a rising edge on this pin can reset the chip. The voltage level after the reset pulse selects the type of interface timing. If the voltage level after the reset pulse stays at HIGH, interface timing for the 68-type microcontroller is selected. If the voltage level after the reset pulse stays at LOW, then interface timing for the 80-type microcontroller is selected.<br><br>Therefore, a positive RESET pulse selects the 80-type microcontroller for interface and a negative RESET pulse selects the 68-type microcontroller for interface.<br><br>The following diagram illustrates the reset pulse and the selected type of microcontroller.<br><br> 

Fig.8 RESET pulse interface timing selection</td></tr>
<tr><td>89</td><td>FR</td><td>I/O</td><td>Frame output or input.<br><br>The frame signal is the AC siganl for generating alternating bias voltage of reverse polarities for LCD cell. When the chip is used as Master in a Master-Slave connection, this pin is an output pin and sends frame signal to the slave. When the chip is used as Slave, this pin is an input pin and accepts frame signal from the master.</td></tr>
<tr><td>90, 91, 92, 94, 95</td><td>V5, V3, V2, V4, V1</td><td>Input</td><td>External LCD Bias voltage.<br><br>The condition VDD≥V1≥V2≥V3≥V4≥V5 must always be met. In addition, $V_{LCD}$ (V5-$V_{DD}$) should not exceed -13 volts.</td></tr>
<tr><td>93</td><td>M/$\overline{S}$</td><td>Input</td><td>Selection for Master or Slave in a master-slave conneciton.<br><br>When this pin is connected to $V_{DD}$ (hardwired-connection), the chip is used as Master. When this pin is connected to $V_{SS}$, the chip is used as Slave.<br><br>
<table>
<tr><td>M/$\overline{S}$</td><td>FR</td><td>COM0-COM15 output</td><td>OSC1</td><td>OSC2</td></tr>
<tr><td>VDD</td><td>Output</td><td>COM0-COM15</td><td>Input</td><td>Output</td></tr>
<tr><td>VSS</td><td>Input</td><td>COM31-COM16</td><td>NC</td><td>Input</td></tr>
</table>
* The common scanning order for the slave driver is reverse to that for master.</td></tr>
</table>

## 4 A SBN1661G_X-BASED DISPLAY SYSTEM

A SBN1661G_X-based display system is shown in Fig. 9.

The SBN1661G_X , on the one side, interfaces with a host microcontroller via address bus , data bus, and control bus. The address bus from the microcontroller needs to be further decoded to generate Chip Select signal. The host microcontroller can perform READ/WRITE operation to the on-chip Display Data Memory, can send commands to the SBN1661G_X, and can program the internal registers to congifure the SBN1661G_X. How data is to be displayed on the LCD panel is completely controlled by the host microcontroller.

On the other side, the SBN1661G_X provides 15 COMMON drivers and 61 SEGMENT drivers to drive the LCD panel.

To expand the COMMON number and SEGMENT number, both the SBN1661G_M18 and SBN1661G_M02 can be used either as a master or as a slave in a master-slave connection. The synchronization between the master and the slave is via the FR (frame) signal and the CL (clock) signal supplied from the master to the slave.

If only segment number needs to be expanded, then the SBN0080G_S18 or the SBN0080G_S02 can be used as slave.

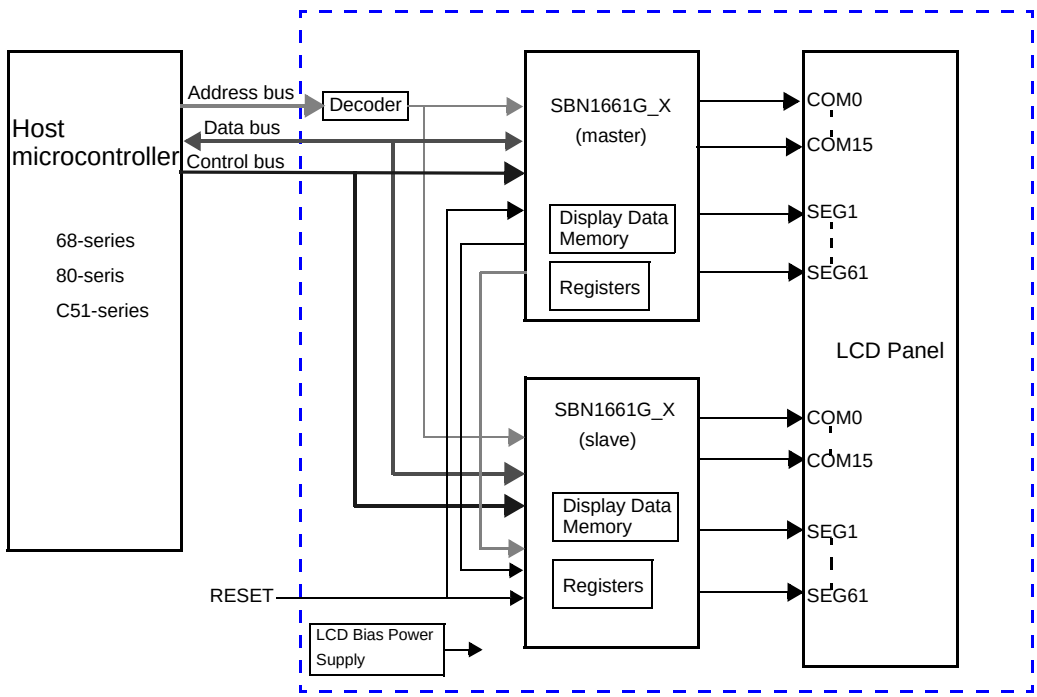



Fig.9 A SBN1661G_X series-based display system

## 5 INTERFACE WITH A HOST MICROCONTROLLER

### 5.1 Selection of interface type by use of the RESET/IF pin(pad)

The SBN1661G_X series can accept two types of interface timing for two types of microconftroller: the 68-type micrcontrollers and the 80-type microcontrollers. Selection of interface type is by use of the dual-function RESET/IF pin(pad). If the voltage at the RESET/IF pin(pad) stays at HIGH after RESET pulse, then the 68-type interface timing is selected. If the voltage at the RESET/IF pin(pad) stays at LOW after RESET pulse, then the 80-type interface timing is selected.

The RESET of the SBN1661G_X is edge-sensitive, instead of level-sensitive. That is, a pulse on the RESET/IF input triggers reset only on the rising edge and falling edge of the pulse. The voltage level after the RESET pulse is used to select interface type.

### 5.2 Interface signal and operation

The interface signal between the host microcontroller and the SBN1661G_X are data bus and control bus. The data bus is an 8-bit (DB0~DB7) bi-directional bus. The control bus is composed of the following siganls: $\overline{C}$/D, E/($\overline{RD}$), and R/$\overline{W}$($\overline{WR}$).

By means of data bus and control bus, the host microcontroller can write data to the on-chip Display Data Memory, can read data from the Display Data Memory, can program the internal registers, can send commands, and can read status of the chip.

It is the host microcontroller's responsibility to put proper data and timing on the data bus and control bus to ensure proper communication.

Table 8 lists the setting for control bus and the types of interface operation.

**Table 8** Interface signal and microcontroller operation

| COMMAN /DATA | 68-type interface | 80-type interface | | Operation |
|---|---|---|---|---|
| $\overline{C}$/D | R/$\overline{W}$ | $\overline{RD}$ | $\overline{WR}$ | |
| 1 | 1 | 0 | 1 | The host microcontroller reads data from the Display Data Memory. |
| 1 | 0 | 1 | 0 | The host microcontroller writes data to the Display Data Memory |
| 0 | 1 | 0 | 1 | The host microcontroller reads the Status Register. |
| 0 | 0 | 1 | 0 | The host microcontroller issues a command or writes data to an internal register. |

### 5.3 Interface Timing

Please refer to Fig. 22 and Fig. 24 for interface timing diagram and Table 42 , Table 43, Table 44, and Table 45 for AC characteristics of interface timing.

### 5.4 Interface Circuit

Please refer to Fig. 24, Fig. 25, and Fig. 26 for interface circuit examples.

## 6 DISPLAY DATA MEMORY AND LCD DISPLAY

The Display Data Memory is a static memory bit(cell) array of 32-row x 80-column. So, the total bit number of the Display Data Memory is 32 x 80 = 2560 bits. Each bit of the memory is mapped to a single pixel (dot) on the LCD panel. A “1” stored in the Display Data Memory bit corresponds to an ON pixel (black dot in normal display) of the LCD panel. A “0” stored in the Display Data Memory bit corresponds to an OFF pixel (background dot in normal display) of the LCD panel.

Column outputs(Column 0~79) of the Display Data Memory is mapped to SEG 0~79 outputs of the SBN1661G_X. The mapping can be normal mapping or inverse mapping. Normal mapping means that Column0 is mapped to SEG0, Column1 to SEG1, Column2 to SEG2, and so on. Inverse mapping means that Column0 is mapped to SEG79, Column1 to SEG78, Column2 to SEG77, and so on. The mapping relation is decided by the Column/Segment Mapping Register.

Any row (80 bits) of the Display Data Memory can be selected as the first row (COM0) to be displayed on the LCD panel. This is decided by the Display Start Line Register. The Display Start Line Register points at the first row of a block of the Display Data Memory, which will be mapped to COM0 of the LCD display. The length of the block of the memory can be 32 rows or 16 rows, which is decided by the Duty Select Register.

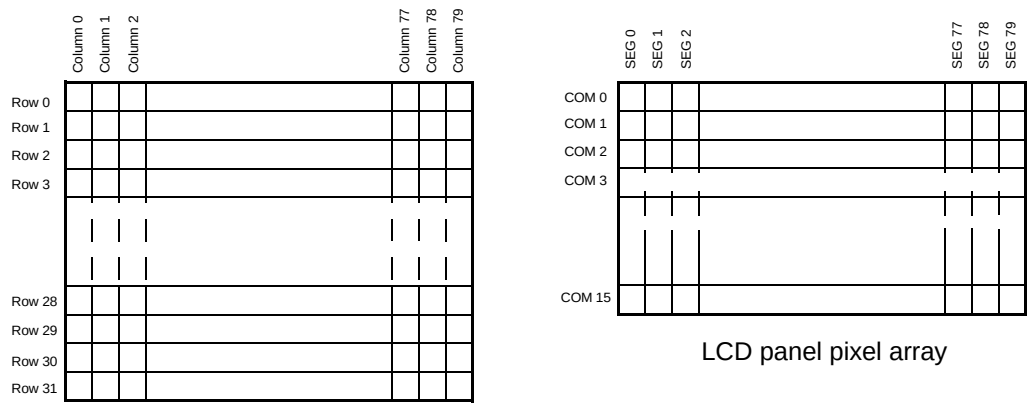



Fig.10 Memory cell array and LCD pixel array

## 7 DISPLAY CONTROL INSTRUCTIONS AND REGISTERS

### 7.1 Registers and their states after hardware RESET

The SBN1661G_X has a set of registers. To ensure proper operation of the devices, these registers must be programmed with proper values after hardware reset.

The registers and their states after RESET is given in Table 9.

**Table 9** Registers and their states after RESET

| Register Name | Description | States after RESET |
|---|---|---|
| Display ON/OFF Register | The Display ON/OFF Register is a 1-bit register. After RESET, its value is LOW and, therefore, the LCD display is turned OFF. | 0 |
| Display Start Line Register | The Display Start Line Register is a 6-bit register. After RESET, its value is 0 0000 and Row0 of the Display Data Memory is mapped to COM0. | 00 0000 |
| Page Addres Register | The Page Address Register is a 2-bit register. After RESET, its value is 11 and, therefore, it points to Page 3 of the Display Data Memory. | 11 |
| Column Address Register | The Column Address Register is a 7-bit register. After RESET, its value is 000 0000 and, therefore, it points to column 0 of the Display Data Memory. | 000 0000 |
| Static Drive ON/OFF Register | The Static Drive ON/OFF Register is a 1-bit register. After RESET, its value is LOW and static display is turned OFF. | 0 |
| Duty Select Register | The Duty Select Register is a 1-bit register. After RESET, its value is HIGH and 1/32 display duty is selected. | 1 |
| Column/Segment Mapping Register | The Column/Segment Mapping Register is a 1-bit register. After RESET, its value is LOW and normal mapping is selected. | 0 |
| Status Register | The Status Register shows the current state of the SBN1661G_X. It is a 4-bit register, with each bit showing the status of a programmed function. | 0000 0000 |

### 7.2 Display ON/OFF and the Display ON/OFF Register

The Display ON/OFF Register is a 1-bit Register. When this bit is progammed to HIGH, the display is turned ON.

When this bit is programmed to LOW, the display is turned OFF. When display is turned OFF, SEG0~SEG60 will stay at either V2 or V3, and COM0~COM15 will stay at their previous value before the Display OFF command is issued.

To program this register, the setting of control bus is given in Table 10 and the setting of the data bus is given in Table 11.

**Table 10** Setting of the control bus for programming the Display ON/OFF Register

| $\overline{C}$/D | E/($\overline{RD}$) | R/$\overline{W}$($\overline{WR}$) |
|---|---|---|
| 0 | 1 | 0 |

**Table 11** Setting of the data bus for programming the Display ON/OFF Register

| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0(LSB) |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | D0 |

When D0=1, the code is AF(Hex) and the display is turned ON. When D0=0, the code is AE(Hex) and the display is turned OFF.

### 7.3 Display Start Line and the Display Start Line Register

The Display Start Line Register is a 5-bit Register. It points at the first row of a block of the Display Data Memory, which will be mapped to COM0. The length of the block of the memory can be 32 rows or 16 rows, which is decided by the Duty Select Register. For example, if the Display Start Line Register is programmed with 00010 ( decimal 2) and display duty is 1/32, then Row2 of the Display Data Memory will be mapped to COM0 of LCD panel, Row3 to COM1, Row4 to COM2, Row30 to COM28, Row31 to COM29, Row0 to COM30, and finally Row1 to COM31, as illustrated in Fig. 11. However, in this case, only Row2~Row17 can be displayed on COM0~COM15, as COM16~COM31 are not availabe from the chip.

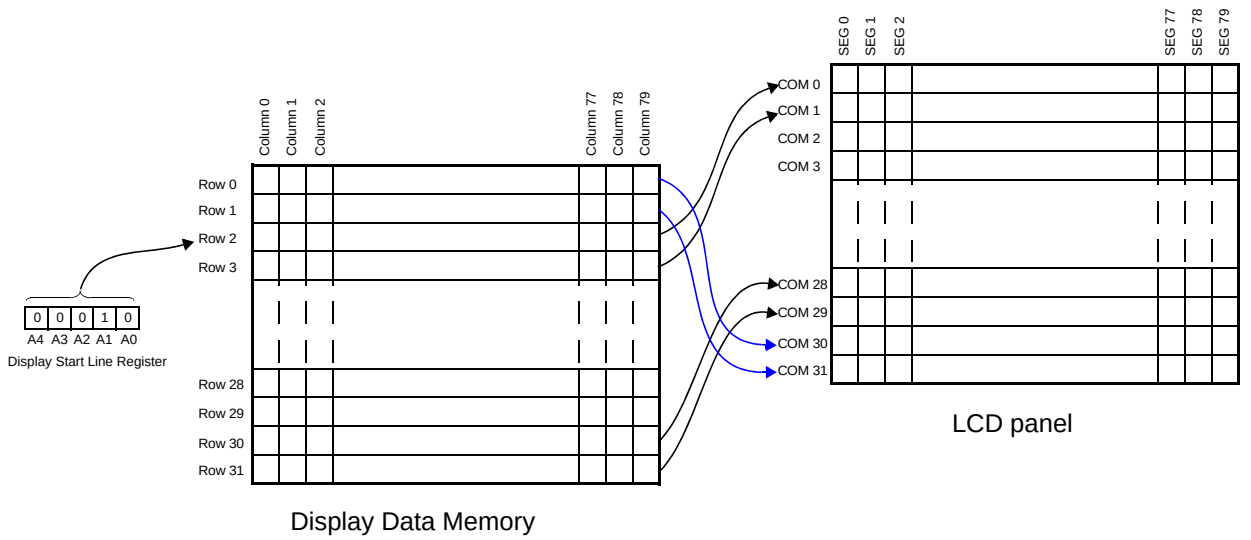



Fig.11 Display Start Line Register

To program this register, the setting of the control bus is given in Table 12 and the setting of the data bus is given in Table 13.

**Table 12** The setting of the control bus for programming the Display Start Line Register

| $\overline{C}$/D | E/($\overline{RD}$) | R/$\overline{W}$($\overline{WR}$) |
|---|---|---|
| 0 | 1 | 0 |

**Table 13** The setting of the data bus for programming the Display Start Line Register

| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0(LSB) |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | A4 | A3 | A2 | A1 | A0 |

A4, A3, A2, A1, and A0 are Start Line address bits and they can be programmed with a value in the range from 0 to 31. Therefore, the code can be from 1100 0000 (C0 Hex) to 1101 1111 (DF Hex).

### 7.4 Display Data Memory Page and the Page Address Register

The on-chip Display Data Memory is divided into 4 pages: Page 0, Page 1, Page 2, and Page 3, with each page having 80 bytes in horizontal direction. Page 0 is from Row 0 to Row 7, Page 1 from Row 8 to Row 15, Page 2 from Row 16 to Row 23, and Page 3 from Row 24 to Row 31, as shown in Fig 12. When the host microtroller intends to perform a READ/WRITE operation to the Display Data Memory, it has to program the Page Adrress Register to indicate which page it intends to access.

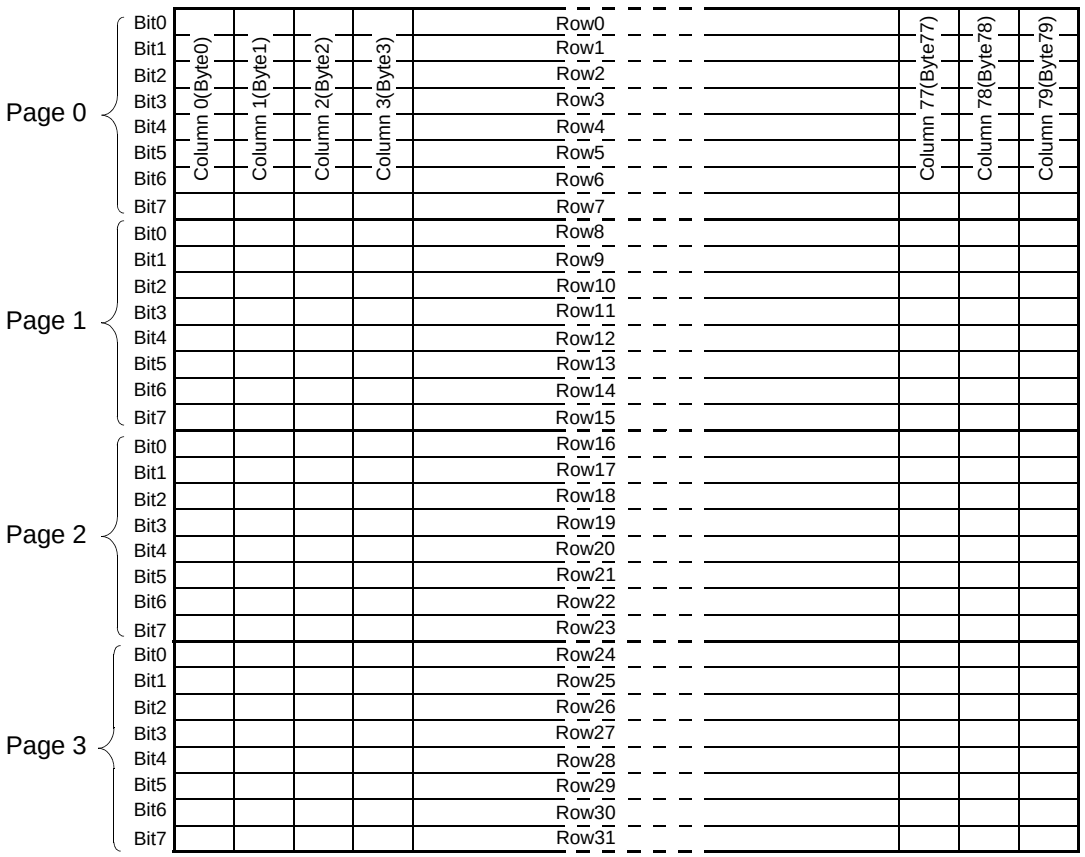



Fig.12 Page/Column allocation of the Display Data Memory

To program this register, the setting of the control bus is given in Table 14 and the setting of the data bus is given in Table 15.

**Table 14** The setting of the control bus for programming the Page Address Register

| $\overline{C}$/D | E/($\overline{RD}$) | R/$\overline{W}$($\overline{WR}$) |
|---|---|---|
| 0 | 1 | 0 |

**Table 15** The setting of the data bus for programming the Page Address Register

| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0(LSB) |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 1 | 0 | A1 | A0 |

A1and A0 are page address bits and can be programmed with a value in the range from 0 to 3. A1A0=00 selects Page 0, A1A0=01 selects Page 1, A1A0=10 selects Page 2, and A1A0=11 selects Page 3. Therefore, the code can be from 1011 1000 (B8 Hex) to 1011 1011 (BB Hex).

### 7.5 Column address and the Column Address Register

The Column Address Register points at a column of the Display Data Memory which the host microcontroller intends to perform a READ/WRITE operation. The Column Address Register automatically increments by 1 after a READ or WRITE operation is finished. When the Column Address Register reaches 79, it overflows to 0. Please refer to Fig.12 for the column sequence in a page of the Display Data Memory.

To program this register, the setting of the control bus is given in Table 16 and the setting of the data bus is given in Table 17.

**Table 16** The setting of the control bus for programming the Column Address Register

| $\overline{C}$/D | E/($\overline{RD}$) | R/$\overline{W}$($\overline{WR}$) |
|---|---|---|
| 0 | 1 | 0 |

**Table 17** The setting of the data bus for programming the Column Address Register

| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0(LSB) |
|---|---|---|---|---|---|---|---|
| 0 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

A6~A0 are column address bits and can be programmed with a value in the range from 0 to 79. Therefore, the code can be from 0000 0000 (00 Hex) to 0100 1111 (4F Hex).

### 7.6 Mapping between Memory Cloumns and Segments and the Column/Segment Mapping Register

The Column/Segment Mapping Register is a 1-bit register and selects the mapping relation between the column outputs of the Display Data Memory and the Segment outputs SEG0~SEG79.

If this register is programmed with HIGH, then the data from column 79 of the Display Data Memory will be output from SEG0. This type of mapping is called *inverted mapping*.

If this register is programmed with LOW, then data from column 0 of the Display Data Memory will be output from SEG0. This type of mapping is called *normal mapping*.

By use of this register, the flexibility of component placement and routing on a PCB can be increased.

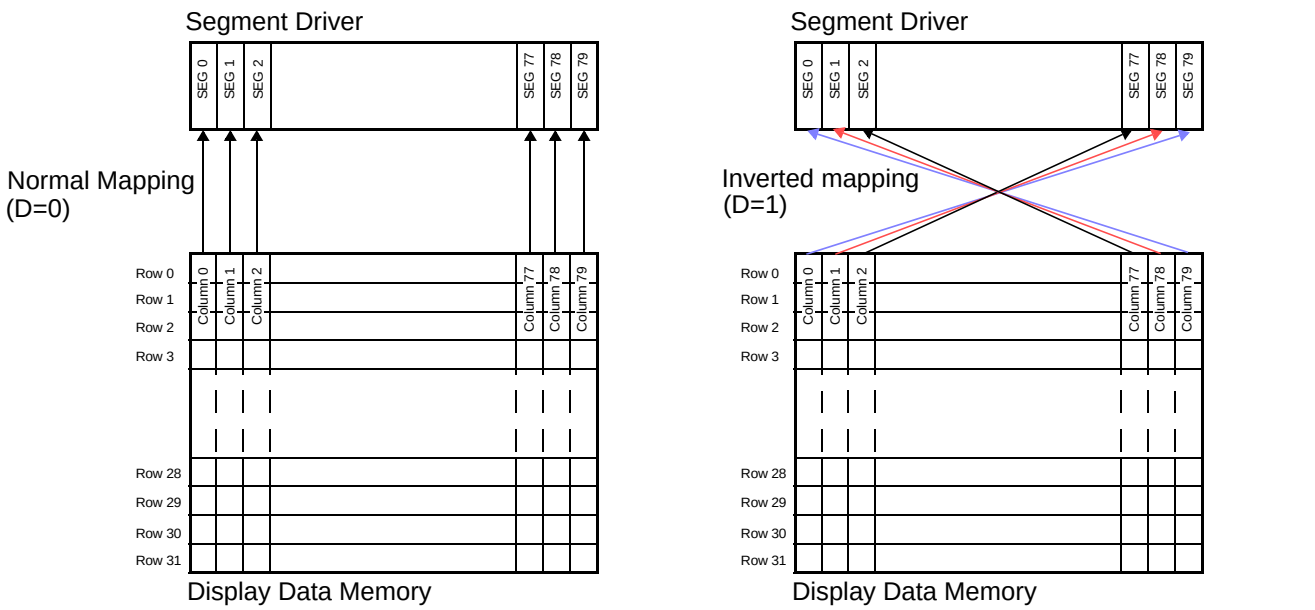



Fig.13 Column/Segment Mapping Register.

To program this register, the setting of the control bus is given in Table 18 and the setting of the data bus is given in Table 19.

**Table 18** The setting of the control bus for programming the Column/Segment Mapping Register

| $\overline{C}$/D | E/($\overline{RD}$) | R/$\overline{W}$($\overline{WR}$) |
|---|---|---|
| 0 | 1 | 0 |

**Table 19** The setting of the data bus for programming the Memory/Segment Mapping Register

| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0(LSB) |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | D |

The least significant bit D can be programmed with either 0 or 1. Therefore, the codes are A0 Hex or A1 Hex.

### 7.7 Static Drive ON/OFF and the Static Drive ON/OFF register

The Static Drive ON/OFF Register is a 1-bit register. It is used to turn ON or OFF the *Static Drive Mode* of the SBN1661G_X.

When this register is programmed with HIGH, *Static Drive Mode* is turned ON and the device enters into *Static Drive Mode*, in which the internal clock circuitry is disabled and the switching of the internal logic is suspended. When this register is programmed with LOW, *Static Drive Mode* is turned OFF and the chip returns to normal operation.

This register is used in combination with the Display ON/OFF register to make the current consumption of the LCD module reduced to almost static level. By turning OFF the display and turning ON the static drive mode,the chip is configured into the following state:

- all COMMON and SEGMENT outputs are set to $V_{DD}$,
- on-chip oscillator or external clock is inhibited and internal logic circuit stays idle,
- OSC2 is in floating state (please refer to Section 11 , On-chip RC Oscillator), and
- the state of registers and the data of the Display Data Memory are kept unchanged.

In addition to turning ON the static drive mode and turning OFF the display, to really reduce the power consumption of the LCD module, the host microcontroller should also send out a power-save signal to turn off the PNP transistor in the bias circuit, such that the current flow from $V_{DD}$ to $V_{EE}$ can be cut off, as shown in Fig. 14.

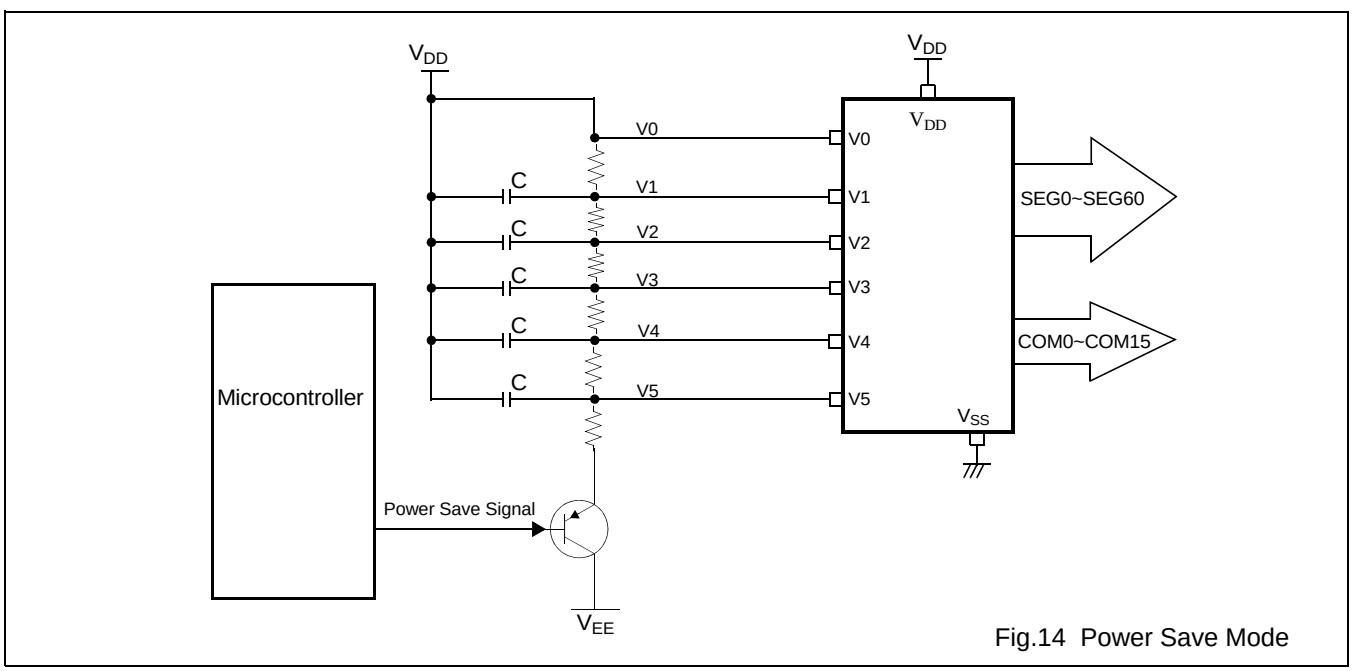



Fig.14 Power Save Mode

To program this register, the setting of the control bus is given in Table 20 and the setting of the data bus is given in Table 21.

**Table 20** The setting of the control bus for programming the Static Drive ON/OFF Register

| $\overline{C}$/D | E/($\overline{RD}$) | R/$\overline{W}$($\overline{WR}$) |
|---|---|---|
| 0 | 1 | 0 |

**Table 21** The setting of the data bus for programming the Static Drive ON/OFF Register

| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0(LSB) |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | D |

The least significant bit D0 can be programmed with either 0 or 1. Therefore, the code is A4 Hex or A5 Hex.

### 7.8 Select Duty and the Select Duty Register

The Select Duty Register is a 1-bit register. If it is programmed with HIGH, 1/32 display duty is selected. If it is programmed with LOW, 1/16 display duty is selected.

To program this register, the setting of the control bus is given in Table 22 and the setting of the data bus is given in Table 23.

**Table 22** The setting of the control bus for programming the Select Duty Register

| $\overline{C}$/D | E/($\overline{RD}$) | R/$\overline{W}$($\overline{WR}$) |
|---|---|---|
| 0 | 1 | 0 |

**Table 23** The setting of the data bus for programming the Select Duty Register

| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0(LSB) |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | D |

The least significant bit D can be programmed with either 0 or 1. Therefore, the code is A8 Hex or A9 Hex.

In a Master-Slave connection using the SBN1661G_M18 or the SBN1661G_M02 as the master, COM0~COM15 will be from the master and COM16~COM31 will be from the slave. The Select Duty Register of both the Master and the Slave should be programmed with HIGH to select 1/32 duty. Fig.15 shows the COMMON sequence of this connection.

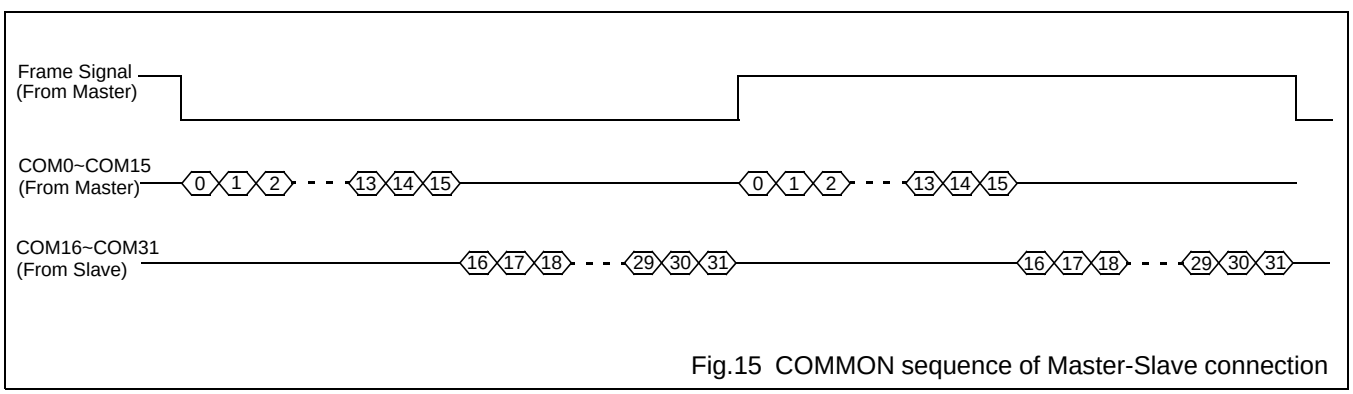



Fig.15 COMMON sequence of Master-Slave connection

This register is not available in the SBN0080G_S18 and the SBN0080G_S02, because both the devices are purely Segment Drivers and their duty cycle is decided by the FR and the CL from the master.

### 7.9 Status Read and Status Register

The Status Register shows the current state of the SBN1661G_X. It can be read by the host microcontroller. Bit 7~4 shows the status and Bit 3~0 are always fixed at 0.

To read the Status Register, the setting of the control bus is given in Table 24, the bit allocation is given in Table 25 and the description for each bit is given in Table 26.

**Table 24** The setting of the control bus for reading the Status Register

| $\overline{C}$/D | E/($\overline{RD}$) | R/$\overline{W}$($\overline{WR}$) |
|---|---|---|
| 0 | 0 | 1 |

**Table 25** The Status Register bit allocation

| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0(LSB) |
|---|---|---|---|---|---|---|---|
| BUSY | MAPPING | ON/OFF | RESET | 0 | 0 | 0 | 0 |

**Table 26** The Status Register bit description

| Bit | Description |
|---|---|
| BUSY | BUSY=1 indicates that the SBN1661G_X is currently busy and can not accept new command or data. The SBN1661G_X is executing a command or is in the process of reset.<br>BUSY=0 indicates that the SBN1661G_X is not busy and is ready to accept new command or data. |
| MAPPING | MAPPING=1 indicates that the Column/Segment Mapping Register has been programmed with a value of “1” and the SEG0 is mapped to Column 79 of the Display Data Memory (inverted mapping).<br>MAPPING=0 indicates that the Column/Segment Mapping Register has been programmed with a value of “0” and the SEG0 is mapped to Column 0 of the Display Data Memory (normal mapping). |
| ON/OFF | The ON/OFF bit indicates the current of status of display.<br>If ON/OFF=0, then the display has been turned ON.<br>If ON/OFF=1, then the display has been turned OFF.<br>Note that the polarity of this bit is inverse to that of the Display ON/OFF Register. |
| RESET | RESET=1 indicates that the SBN1661G_X is currently in the process of being reset.<br>RESET=0 indicates that the SBN1661G_X is currently in normal operation. |

## 8 COMMANDS

The host microcontroller can issue commands to the SBN1661G_X. Table 27 lists all the commands. When issuing a command, the host microcontroller should put the command code on the data bus. The host microcontroller should also give the control bus C/D, E(RD), and R/W(WR) proper value and timing.

**Table 27** Commands

| COMMAND | COMMAND CODE | | | | | | | | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| Write Display Data | Data to be written into the Display Data Memory. | | | | | | | | Write a byte of data to the Display Data Memory. |
| Read Display Data | Data read from the Display Data Memory. | | | | | | | | Read a byte of data from the Display Data Memory. |
| Read-Modify-Write | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Start Read-Modify-Write operation. |
| END | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | Stop Read-Modify-Write operation. |
| Software Reset | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | Software Reset. |

### 8.1 Write Display Data

The Write Display Data command writes a byte (8 bits) of data to the Display Data Memory. Data is put on the data bus by the host microcontroller. The location which accepts this byte of data is pointed to by the Page Address Register and the Column Address Register. At the end of the command operation, the content of the Column Address Register is automatically incremented by 1.

For page address and column address of the Display Data Memory, please refer to Fig. 12.

Table 28 gives the control bus setting for this command.

**Table 28** The setting of the control bus for issuing Write Display Data command

| C/D | E/(RD) | R/W(WR) |
|---|---|---|
| 1 | 1 | 0 |

### 8.2 Read Display Data

The Read Display Data command starts a 3-step operation.

1. First, the current data of the internal 8-bit output latch of the Display Data Memory is read by the microcontroller, via the 8-bit data bus DB0~DB7.
2. Then, a byte of data of the Display Data Memory is transferred to the 8-bit output latch from a location specified by the Page Address Register and the Column Address Register,
3. Finally, the content of the Column Address Register is automatically incremented by one.

Fig. 16 shows the internal 8-bit ouptut latch located between the 8-bit I/O data bus and the Display Data Memory cell array. Because of this internal 8-bit output latch, a dummy read is needed to obtain correct data from the Display Data Memory.

For Display Data Write operation, a dummy write **is not** needed, because data can be directly written from the data bus to internal memory cells.

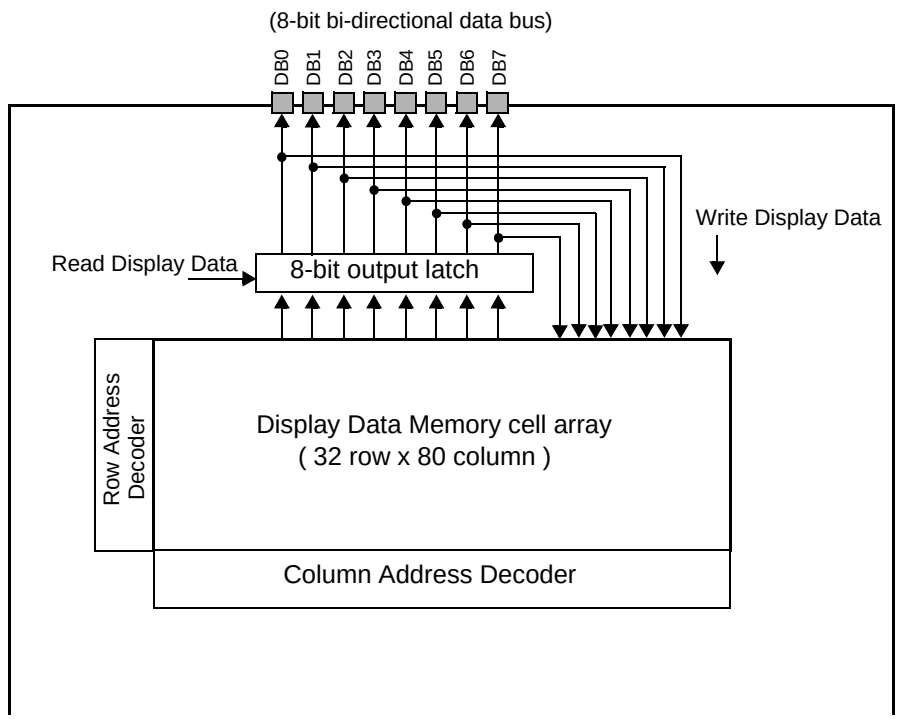



Fig.16 Read Display Data Memory

Table 29 gives the control bus setting for this command.

**Table 29** The setting of the control bus for issuing Read Display Data command

| $\overline{C}$/D | E/($\overline{RD}$) | R/$\overline{W}$($\overline{WR}$) |
|---|---|---|
| 1 | 0 | 1 |

### 8.3 Read-Modify-Write

When the Read-Modify-Write command is issued, the SBN1661G_X enters into Read-Modify-Write mode.

In normal operation, when a Read Display Data command or a Write Display Data command is issued, the content of the Column Address Register is automatically incremented by one after the command operation is finished. However, during Read-Modify-Write mode, the content of the Column Address Register is not incremented by one after a Read Display Data command is finished; only the Write Display Data command can make the content of the Column Address Register automatically incremented by one after the command operation is finished.

During Read-Modify-Write mode, any other registers, except the Column Address Register, can be modified. This command is useful when a block of the Display Data Memory needs to be repeatedly read and updated.

Fig. 17 gives the change sequence of the Column Address Register during Read-Modify-Write mode. Figure 18 gives the flow chart for Read-Modify-Write command.

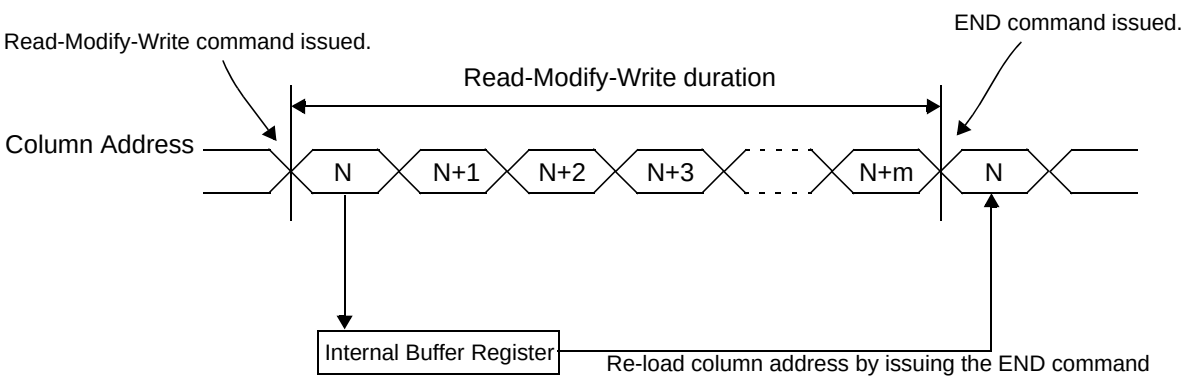



Fig.17 Column address change during Read-Modify-Write

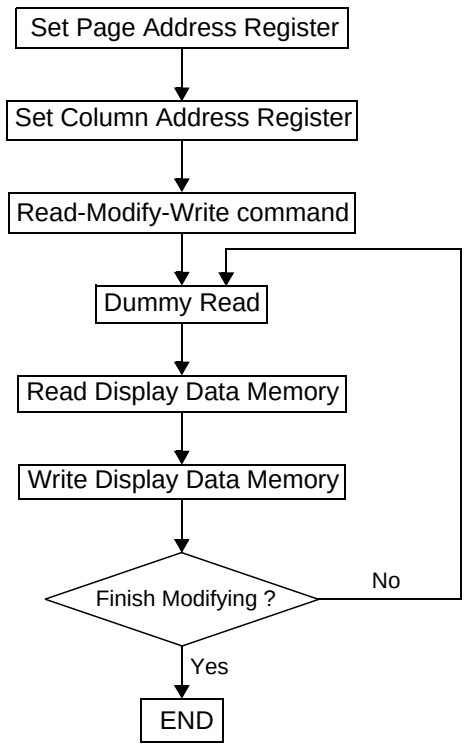



Fig.18 The flowchart for Read-Modify-Write

Table 30 gives the setting for the control bus and the setting of the data bus is given in Table 31.

**Table 30** The setting of the control bus for the Read-Modify-Write command

| $\overline{C}$/D | E/($\overline{RD}$) | R/$\overline{W}$($\overline{WR}$) |
|---|---|---|
| 0 | 1 | 0 |

**Table 31** The setting of the data bus for the Read-Modify-Write command

| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0(LSB) |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

The command code is E0 Hex.

### 8.4 The END command

The END command releases the Read-Modify-Write mode and re-loads the Column Address Register with the value previously stored in the internal buffer (refer to Fig. 17) when the Read-Modify-Write command was issued.

Table 32 gives the setting for the control bus and the setting of the data bus is given in Table 33.

**Table 32** The setting of the control bus for the END command

| $\overline{C}$/D | E/($\overline{RD}$) | R/$\overline{W}$($\overline{WR}$) |
|---|---|---|
| 0 | 1 | 0 |

**Table 33** The setting of the data bus for the END command

| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0(LSB) |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |

The command code is EE Hex.

### 8.5 Software RESET command

The Software Reset command is different from the hardware reset and can not be used to replace hardware reset.

When Software Reset is issued by the host microcontroller,

- the content of the Display Start Line Register is cleared to zero(A4~A0=00000),
- the Page Address Register is set to 3 (A1 A0 = 11),
- the content of the Display Data Memory remains unchanged, and
- the content of all other registers remains unchanged.

Table 34 gives the setting for the control bus and the setting of the data bus is given in Table 35.

**Table 34** The setting of the control bus for Software RESET

| $\overline{C}$/D | E/($\overline{RD}$) | R/$\overline{W}$($\overline{WR}$) |
|---|---|---|
| 0 | 1 | 0 |

**Table 35** The setting of the data bus for Software RESET

| D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0(LSB) |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |

The command code is E2 Hex.

## 9 LCD BIAS CIRCUIT

A typical LCD bias circuit is shownin Fig. 19. The condition VDD≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5 must always be met. The maximum allowed voltage for LCD bias ($V_{LCD}$=$V_{DD}$-$V_5$) should not exceed 13 volts.

| COMPONENT | RECOMMENDED VALUE |
|---|---|
| C | 0.1 μF, electrolytic |
| R1 | 2.2K |
| R2 | 7.5K |
| R3 | 10K |
| TR1 | PNP |

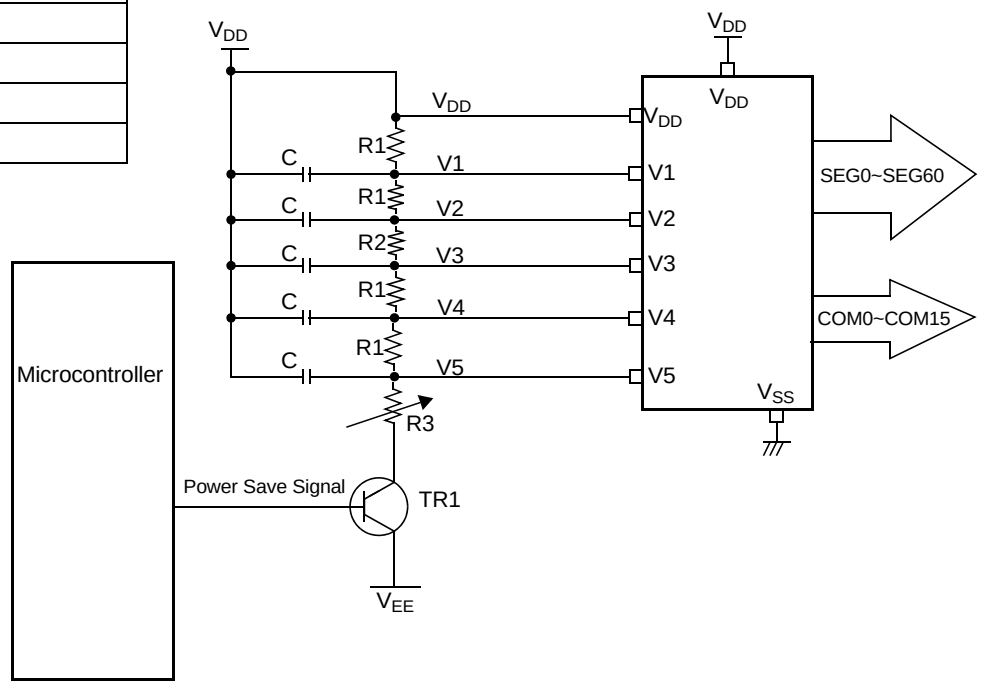



Fig.19 LCD Bias circuit

## 10 COMMON, SEGMENT OUTPUT VOLTAGE

The output voltage level of COMMON driver and SEGMENT driver is given in Table 36.

The output voltage level of COMMON driver is decided by the combination of Frame signal, internal COMMON COUNTER output, and the Display ON/OFF register.

The output voltage level of SEGMENT driver is decided by the combination of Frame signal, Display Data, and the Display ON/OFF register.

**Table 36** COMMON/SEGMENT ouptut voltage level

| FR | Data | DISPLAY ON/OFF | SEG0~SEG60 (SEG0~SEG79) | COM0~COM15 |
|---|---|---|---|---|
| L | L | ON | V3 | V4 |
| L | H | ON | V5 | $V_{DD}$ |
| H | L | ON | V2 | V1 |
| H | H | ON | $V_{DD}$ | V5 |
| x(don't care) | x(don't care) | OFF | V2 or V3 | previous voltage |

Note that, in the above table, "Data" for the COM0~COM15 is actually the output of the internal COMMON COUNTER, which generates horizontal raster scanning signal.

During RESET, both SEGMENT and COMMON outputs are at $V_{DD}$.

## 11 ON-CHIP RC OSCILLATOR

The SBN1661G_M18 has an on-chip RC-type oscillator. All other three members of the family do not have on-chip oscillator and need external clock source. The output CLK of the oscillator is the basic timing clock of the internal control logic, display pixel rate, and is also used to generate frame signal.

The capacitor of the RC-oscillator is fabricated on-chip. Only an external resistor Rf needs to be connected across OSC1 and OSC2. The recommended value of Rf is in the range from 1000K ohm to 1200K ohm. During PCB layout, this resistor should be placed as close to the SBN1661G_M18 as possible, such that stray capacitance, inductance, and resistance can be minimized.

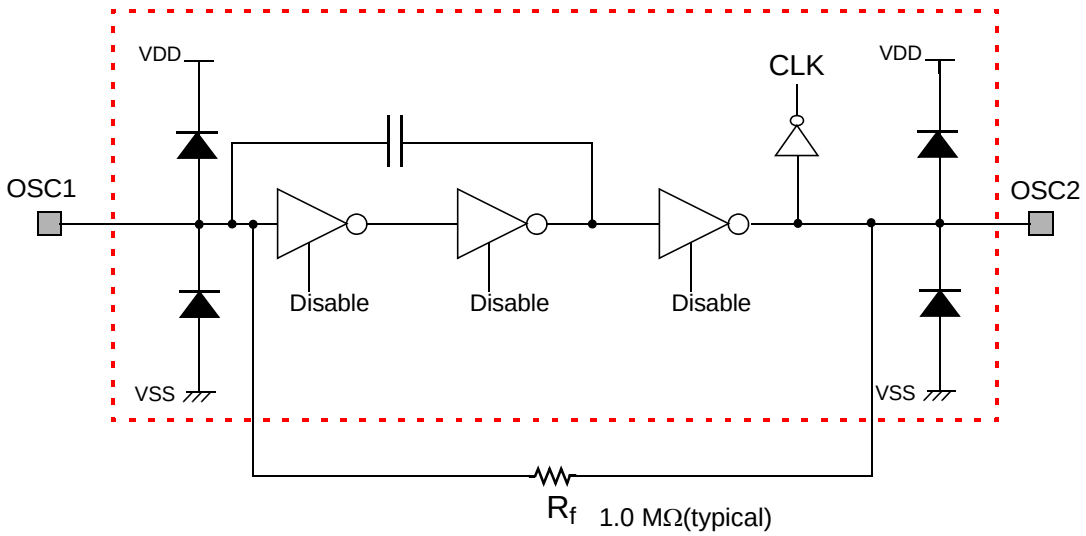



Fig.20 On-chip RC oscillator

The characteristics of the oscillator is given is Table. 37.

**Table 37** On-chip RC oscillator characteristics, $T_{amb}$ = −20 to +75 °C

| **Oscillation** | **min.** | **typ.** | **max.** | **unit** |
|---|---|---|---|---|
| Oscillation frequency at $V_{DD}$=5V, $R_f$= 1.0 MΩ ±20% | 17.6 | 21.5 | 25.9 | KHz |
| Oscillation frequency at $V_{DD}$=3V, $R_f$= 1.0 MΩ ±20% | 15.7 | 19.1 | 22.8 | KHz |

## 12 ELECTRICAL CHARACTERISTICS

### 12.1 Absolute maximum rating

**Table 38** Absolute maximum rating

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | voltage on the $V_{DD}$ pin(pad) | −0.3 | +7.0 | Volts |
| $V_{LCD}$ (note 2) | LCD bias voltage, $V_{LCD}$=$V_{DD}$-V5 | 3.5 | 13 | Volts |
| $V_I$ | input voltage on any pin with respect to $V_{SS}$ | −0.3 | $V_{DD}$ + 0.3 | Volts |
| $P_D$ | power dissipation | | 250 | mW |
| $T_{stg}$ | storage temperature range | −55 | +125 | °C |
| $T_{amb}$ | operating ambient temperature range | -40 | + 85 | °C |
| Tsol (note 3) | soldering temperature/time at pin | | 260 °C,<br>10 Second | |

**Notes**

1. The following applies to the Absolute Maximum Rating:
   a) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.
   b) The SBN1661G_X series includes circuitry specifically designed for the protection of its internal devices from the damaging effect of excessive static charge (ESD). However, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
   c) Parameters are valid over operating temperature range unless otherwise specified.
   d) All voltages are with respect to $V_{SS,}$ unless otherwise noted.
2. The condition VDD≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5 must always be met.
3. QFP-type packages are sensitive to moisture of the enviroment, please check the drypack indicator on the tray package before soldering. Exposure to moisture longer than the rated drypack level may lead to cracking of the plastic package or broken bonding wiring inside the chip.

## 13 DC CHARACTERISTICS

**Table 39** DC Characteristics

$V_{DD}$ = 5 V ±10%; $V_{SS}$ = 0 V; all voltages with respect to $V_{SS}$, unless otherwise specified; $T_{amb}$ = −20 to +75 °C.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage for logic | | 2.7 | 5.0 | 5.5 | V |
| $V_{LCD}$ | LCD bias voltage $V_{LCD}$= $V_{DD}$-V5 | | 3.5 | | 13 | V |
| $V_{IL}$ | LOW level input voltage | For all inputs | 0 ~ 0.7 @vdd=2.7 | 0 ~ 1.1 @vdd=5.0 | 0 ~ 1.2 @vdd=5.5 | V |
| $V_{IH}$ | HIGH level input voltage | For all inputs | 2.0 ~ 2.7 @vdd=2.7 | 3.5 ~ 5.0 @vdd=5.0 | 3.7 ~ 5.5 @vdd=5.5 | V |
| $V_{OL}$ | LOW level output voltage | For all outputs | 0.0 | | 0.3 | V |
| $V_{OH}$ | HIGH level output voltage | For all outputs | $V_{DD}$ - 0.3 | | $V_{DD}$ | V |
| $I_{STBY}$ | Standby current at $V_5$=-5 volts | Note 1 | | | 3.0 | µA |
| $I_{DD(1)}$ | Operating current at $V_5$=-5 volts and $f_{CL}$=2KHz, $V_{LCD}$=10 volts | Note 2 & Note 3 | | 2.7 | 5.6 | µA |
| $I_{DD(2)}$ | Operating current at $V_5$=-5 volts and Rf=1 MΩ, $V_{LCD}$=10 volts | | | 12.3 | 15.6 | µA |
| $I_{DD(3)}$ | Operating current at $V_5$=-5 volts and $f_{CL}$=21.8 KHz, $V_{LCD}$=10 volts | | | 5.3 | 10.8 | µA |
| $I_{DD(4)}$ | Operating current at $V_5$=-5 volts and $t_{CYC}$=100 KHz, $V_{LCD}$=10 volts | Note 4 | | 21.7 | 26.2 | µA |
| $f_{osc(VDD=5V)}$, $f_{osc(VDD=3V)}$ | Please refer to Table 37, On-chip RC oscillator characteristics. | | | | | |
| $C_{in}$ | Input capacitance of all input pins | | | 5.0 | 8.0 | pF |
| $R_{ON}$ | LCD driver ON resistance | Note 5 | | 5.0 | 7.5 | KΩ |
| $t_R$ | Reset time | Note 6 | 1.0 | | | µS |

**Notes:**

1. Conditions for the measurement: OSC1=OSC2=VDD, measured at the $V_{DD}$ pin.
2. These values are measured when the microcontroller does not perform any READ/WRITE operation to the chip.
3. These meaurements are for different members of the series:
   a) $I_{DD(1)}$ are measured for the SBN1661G_M02 and the SBN0080G_S02,
   b) $I_{DD(2)}$ are measured for the SBN1661G_M18, and
   c) $I_{DD(3)}$ are measured for the SBN0080G_S18.
4. These values are measured when the microcontroller continuously performs READ/WRITE operation to the chip.
5. This measurement is for the transmission high-voltage PMOS or NMOS of COM0~15 and SEG0~60(79). Please refer to Section 18 for these driver circuit. The meaurement is for the case when the voltage differential between the source and the drain of the high voltage PMOS or NMOS is 0.1 volts.
6. The value is relative to the RESET pulse edge. That is, 1.0 µS after the last RESET edge, the device is completely reset.

## 14 AC TIMING CHARACTERISTICS

### 14.1 CL and FR timing

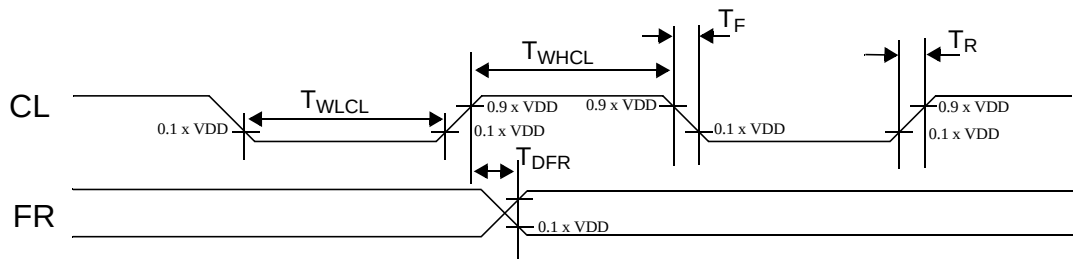



Fig.21 Display Control Signal Timing

**Table 40** CL and FR timing characteristics at $V_{DD}$=5 volts

$V_{DD}$ = 5 V ±10%; $V_{SS}$ = 0 V; all voltages with respect to $V_{SS}$ unless otherwise specified; $T_{amb}$ = −20 to +75 °C.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $T_{WHCL}$ | CL clock high pulse width | | 33 | | | µs |
| $T_{WLCL}$ | CL cock low pulse width | | 33 | | | µs |
| $T_R$ | CL clock rise time | | | 28 | 120 | ns |
| $T_F$ | CL clock fall time | | | 28 | 120 | ns |
| $T_{DFR(input)}$ | FR delay time (input) | When used as input in Slave Mode application | -2.0 | 0.2 | 1.6 | µS |
| $T_{DFR(output)}$ | FR delay time (output) | When used as output in Master Mode application, with CL= 100 pF. | | 0.2 | 0.36 | µS |

**Table 41** CL and FR timing characteristics at $V_{DD}$=3 volts

$V_{DD}$ = 3 V ±10%; $V_{SS}$ = 0 V; all voltages with respect to $V_{SS}$ unless otherwise specified; $T_{amb}$ = −20 to +75 °C.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $T_{WHCL}$ | CL clock high pulse width | | 65 | | | µs |
| $T_{WLCL}$ | CL cock low pulse width | | 65 | | | µs |
| $T_R$ | CL clock rise time | | | 50 | 220 | ns |
| $T_F$ | CL clock fall time | | | 50 | 220 | ns |
| $T_{DFR(input)}$ | FR delay time (input) | When used as input in Slave Mode application | -3.6 | 0.36 | 3.6 | µS |
| $T_{DFR(output)}$ | FR delay time (output) | When used as output in Master Mode application, with CL= 100 pF. | | 0.32 | 0.6 | µS |

### 14.2 AC timing for interface with an 80-type microcontroller

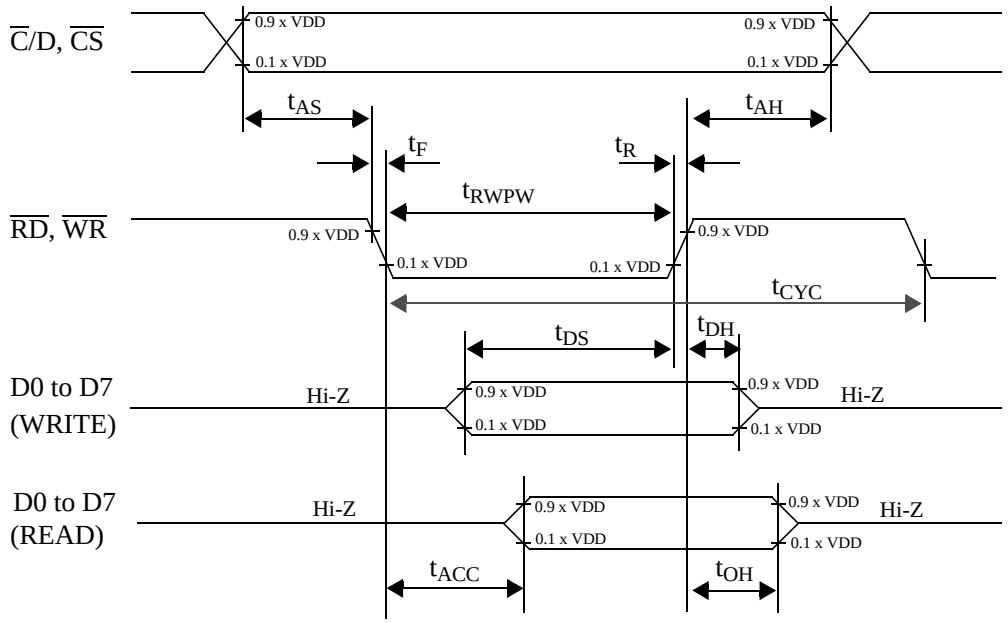



Fig.22 AC timing for interface with a 80-type microcontroller

**Table 42** AC timing for interface with a 80-type microcontorller at $V_{DD}$=5 volts

$V_{DD}$ = 5 V ±10%; $V_{SS}$ = 0 V; $T_{amb}$ = -20 °C to +75°C.

| symbol | parameter | min. | max. | test conditons | unit |
|---|---|---|---|---|---|
| $t_{AS}$ | Address set-up time | 20 | | | ns |
| $t_{AH}$ | Address hold time | 10 | | | ns |
| $t_F$, $t_R$ | Read/Write pulse falling/rising time | | 15 | | ns |
| $t_{RWPW}$ | Read/Write pulse width | 200 | | | ns |
| $t_{CYC}$ | System cycle time | 1000 | | | ns |
| $t_{DS}$ | Data setup time | 80 | | | ns |
| $t_{DH}$ | Data hold time | 10 | | | ns |
| $t_{ACC}$ | Data READ access time | | 90 | CL= 100 pF. | ns |
| $t_{OH}$ | Data READ output hold time | 10 | 60 | Refer to Fig. 23. | ns |

**Table 43** AC timing for interface with an 80-type microcontorller at $V_{DD}$=3 volts

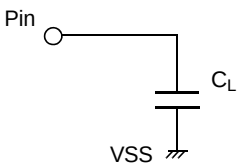
$V_{DD}$ = 3 V ±10%; $V_{SS}$ = 0 V; $T_{amb}$ = -20 °C to +75°C.

| symbol | parameter | min. | max. | test conditons | unit |
|---|---|---|---|---|---|
| $t_{AS}$ | Address set-up time | 40 | | | ns |
| $t_{AH}$ | Address hold time | 20 | | | ns |
| $t_F$, $t_R$ | Read/Write pulse falling/rising time | | 15 | | ns |
| $t_{RWPW}$ | Read/Write pulse width | 400 | | | ns |
| $t_{CYC}$ | System cycle time | 2000 | | | ns |
| $t_{DS}$ | Data setup time | 160 | | | ns |

| symbol | parameter | min. | max. | test conditons | unit |
|---|---|---|---|---|---|
| $t_{DH}$ | Data hold time | 20 | | | ns |
| $t_{ACC}$ | Data READ access time | | 180 | CL= 100 pF, | ns |
| $t_{OH}$ | Data READ output hold time | 20 | 120 | Refer to 23. | ns |

**Note:**

The measurement is with the load circuit connected. The load circuit is shown in Fig. 23.




$C_L$= 100 pF (including wiring and probe capacitance).

Fig.23 Load circuit.

### 14.3 AC timing for interface with a 68-type microcontroller

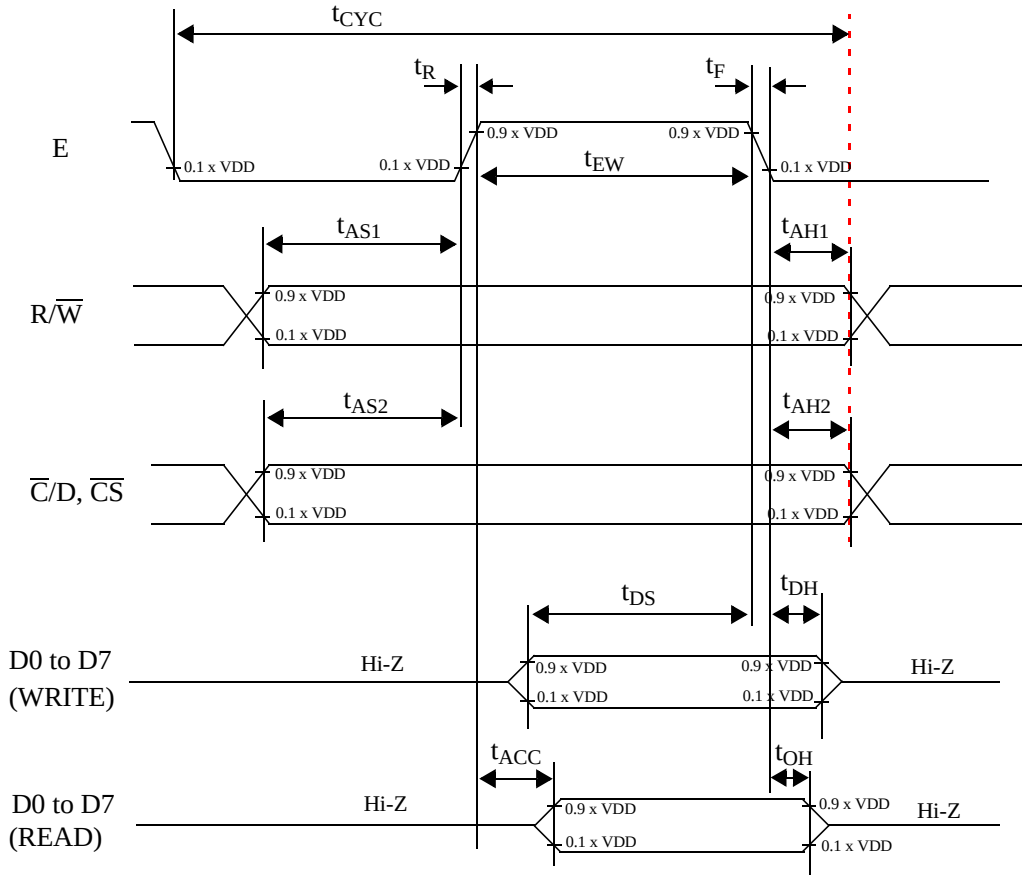



Fig.24 AC timing for interface with a 68-type microcontroller

**Table 44** AC timing for interface with a 68-type microcontroller at $V_{DD}$=5 volts

$V_{DD}$ = 5 V ±10%; $V_{SS}$ = 0 V; $T_{amb}$ = -20 °C to +75°C.

| symbol | parameter | min. | max. | test conditons | unit |
|---|---|---|---|---|---|
| $t_{AS1}$ | Address set-up time with respect to R/$\overline{W}$ | 20 | | | ns |
| $t_{AS2}$ | Address set-up time with respect to $\overline{C}$/D, $\overline{CS}$ | 20 | | | ns |
| $t_{AH1}$ | Address hold time with respect to R/$\overline{W}$ | 10 | | | ns |
| $t_{AH2}$ | Address hold time respect with to $\overline{C}$/D, $\overline{CS}$ | 10 | | | ns |
| $t_F$, $t_R$ | Enable (E) pulse falling/rising time | | 15 | | ns |
| $t_{CYC}$ | System cycle time | 1000 | | Note 1 | ns |
| $t_{EWR}$ | Enable pulse width for READ | 100 | | | ns |
| $t_{EWW}$ | Enable pulse width for WRITE | 80 | | | ns |
| $t_{DS}$ | Data setup time | 80 | | | ns |
| $t_{DH}$ | Data hold time | 10 | | | ns |
| $t_{ACC}$ | Data access time | | 90 | CL= 100 pF. | ns |
| $t_{OH}$ | Data output hold time | 10 | 60 | Refer to Fig. 23. | ns |

**Table 45** AC timing for interface with a 68-type microcontroller at $V_{DD}$=3 volts

$V_{DD}$ = 3 V ±10%; $V_{SS}$ = 0 V; $T_{amb}$ = -20 °C to +75°C.

| symbol | parameter | min. | max. | test conditons | unit |
|---|---|---|---|---|---|
| $t_{AS1}$ | Address set-up time with respect to R/$\overline{W}$ | 40 | | | ns |
| $t_{AS2}$ | Address set-up time with respect to $\overline{C}$/D, $\overline{CS}$ | 40 | | | ns |
| $t_{AH1}$ | Address hold time with respect to R/$\overline{W}$ | 20 | | | ns |
| $t_{AH2}$ | Address hold time respect with to $\overline{C}$/D, $\overline{CS}$ | 20 | | | ns |
| $t_F$, $t_R$ | Enable (E) pulse falling/rising time | | 15 | | ns |
| $t_{CYC}$ | System cycle time | 2000 | | Note 1 | ns |
| $t_{EWR}$ | Enable pulse width for READ | 200 | | | ns |
| $t_{EWW}$ | Enable pulse width for WRITE | 160 | | | ns |
| $t_{DS}$ | Data setup time | 160 | | | ns |
| $t_{DH}$ | Data hold time | 20 | | | ns |
| $t_{ACC}$ | Data access time | | 180 | CL= 100 pF. | ns |
| $t_{OH}$ | Data output hold time | 20 | 120 | Refer to Fig. 23. | ns |

**Note:**

1. The system cycle time($t_{CYC}$) is the time duration from the time when Chip Enable is enabled to the time when Chip Select is released.

## 15 MICROCONTROLLER INTERFACE CIRCUIT

### 15.1 Example for interface with a 80-family microcontroller

Note:
This example is applicable to the SBN1661G_M02.

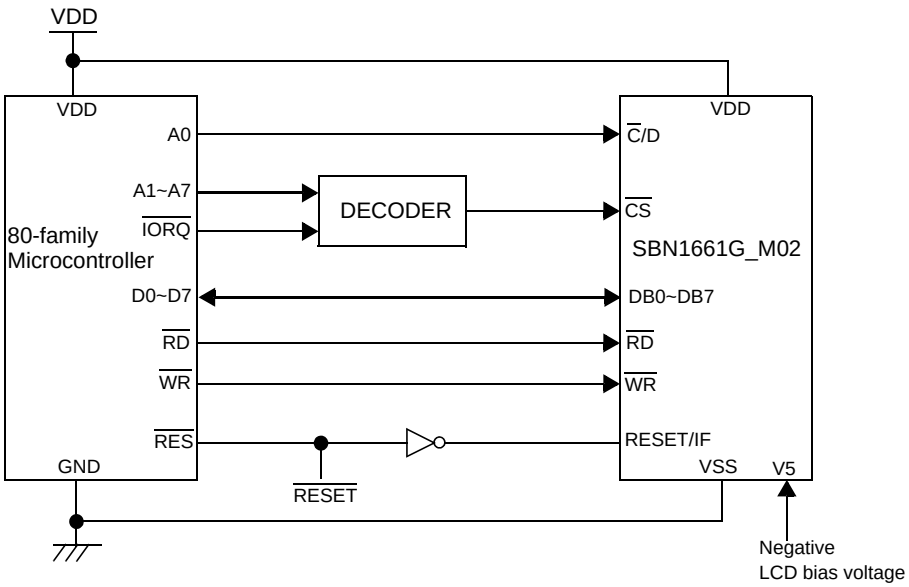



Fig.25 Interface example with an 80-family microcontroller

### 15.2 Example for interface with a 68-family microcontroller

Note:
This example is applicable to the SBN1661G_M02. The $\overline{CS}$ selection for the SBN0080G_S18 and the SBN0080G_S02 can be decoded from the address lines in the same way. For application with the SBN1661G_M18, which does not have a $\overline{CS}$ input, the $\overline{CS}$ output from the decoder must be ORed with $\overline{C}$/D, E, and R/$\overline{W}$.

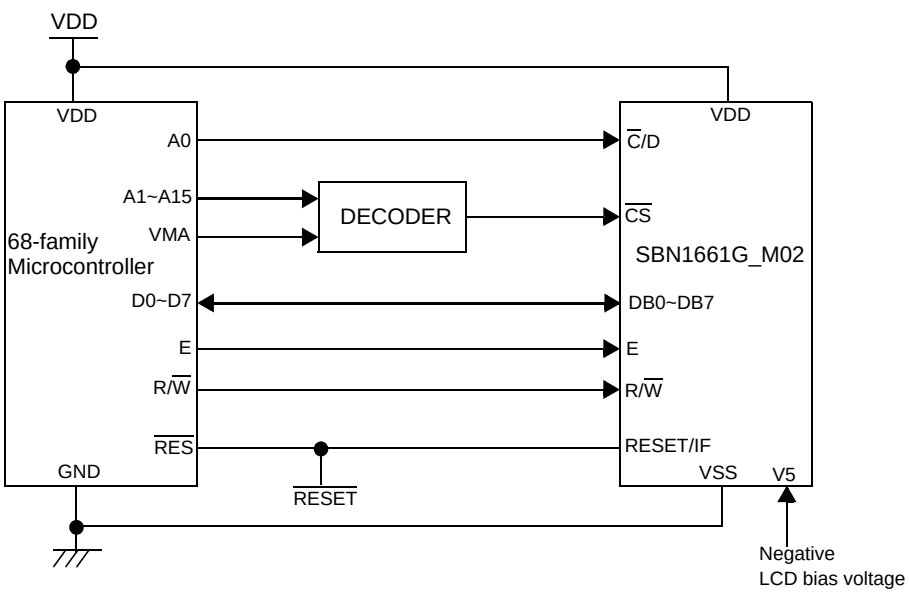



Fig.26 Interface example with a 68-family microcontroller

### 15.3 Example for interface with other types of 8-bit microcontroller

Note:

This example is applicable only to the SBN1661G_M18, which does not have a $\overline{CS}$ input and the $\overline{CS}$ output from the address or I/O space decoding circut must be ORed with $\overline{C}$/D, $\overline{RD}$(E), and ($\overline{WR}$)R/$\overline{W}$.

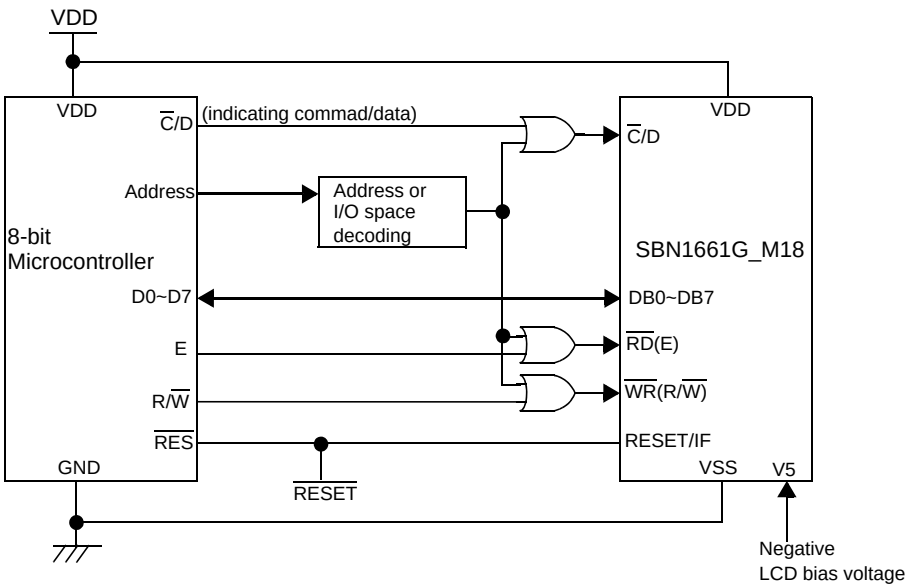



Fig.27 Interface example with an 8-bit microcontroller

## 16 SYNCHRONIZATION OF CLOCK AND FRAME IN MASTER/SLAVE CONNECTIONS

To expand COMMON/SEGMENT number, both the SBN1661G_M18 and the SBN1661G_M02 can be used Master. They can also be used as Slave. However, if the SBN1661G_M02 is used as Master, external clock source is needed, as it has no on-chip oscillator.

In master/slave connections, clock and frame between the master and its slaves must be in synchronization.

The SBN0080G_S18 and the SBN0080G_S02 can be used only as Slave for SEGMENT expansion.

### 16.1 SBN1661G_M18 connected with a SBN1661G_M18

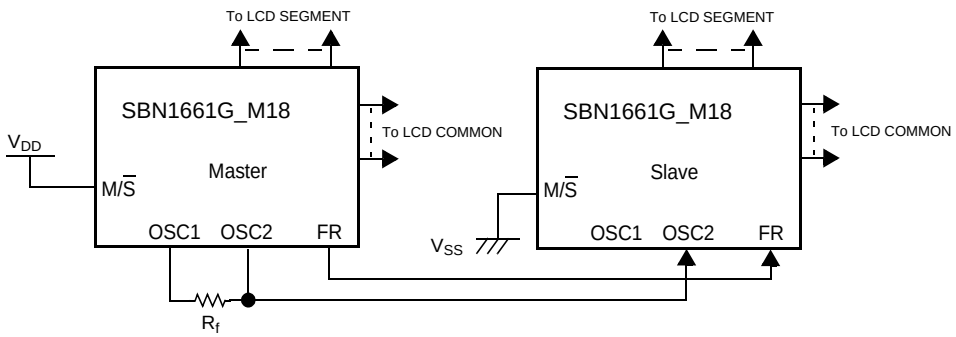
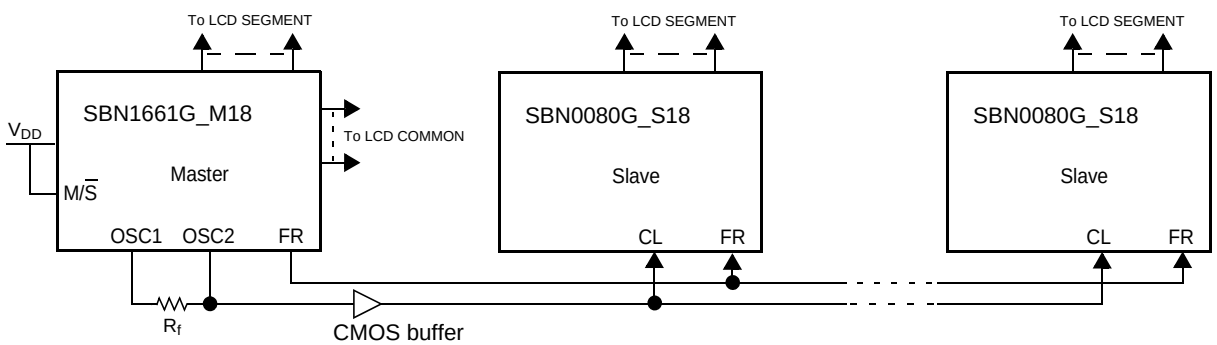



Fig.28 SBN1661G_M18 connected with a SBN1661G_M18.

### 16.2 SBN1661G_M18 connected with more than two SBN0080G_S18




Note: when more than two slaves are connected, a CMOS clock buffer is needed to drive all the slaves. The duty and phase of the clock to all the slaves must be the same as that for the master.

Fig.29 SBN1661G_M18 connected with more than two SBN0080G_S18

### 16.3 SBN1661G_M02 connected with a SBN1661G_M02

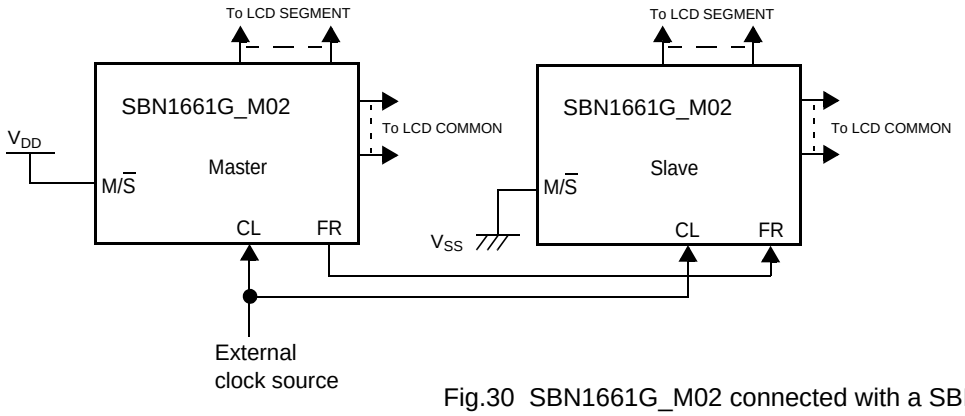



Fig.30 SBN1661G_M02 connected with a SBN1661G_M02.

### 16.4 SBN1661G_M02 connected with a SBN0080G_S02

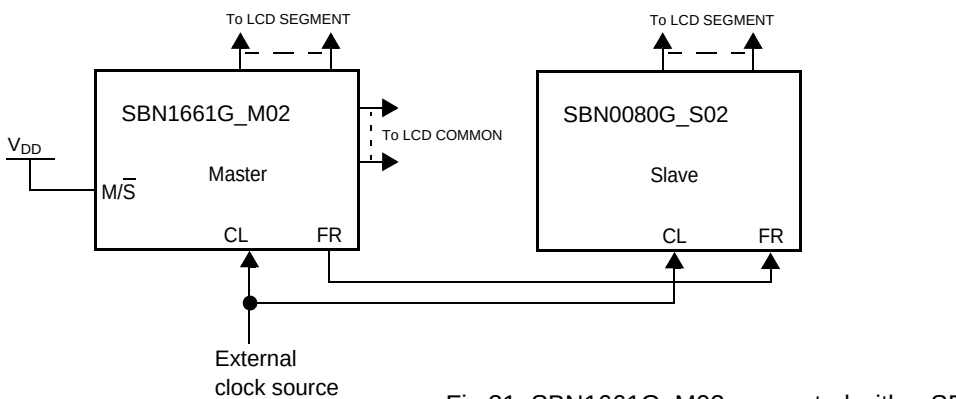



Fig.31 SBN1661G_M02 connected with a SBN0080G_S02.

## 17 TYPICAL APPLICATIONS

### 17.1 1/16 duty, 10 characters x 2 lines

In this application, 10-characters x 2-lines can be displayed, if the format of character font is 6 x 8 pixels.

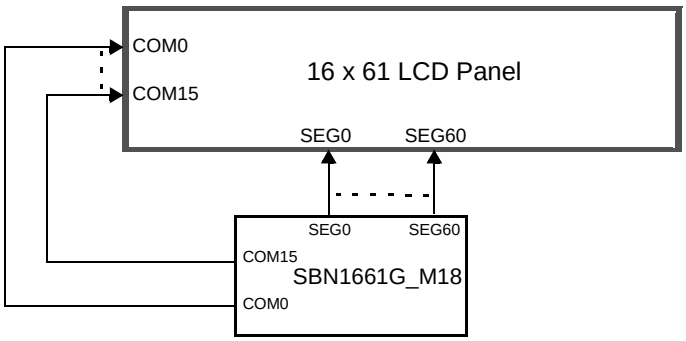



Fig.32 1/16 duty, 10 characters x 2 lines

### 17.2 1/16 duty, 23 characters x 2 rows

In this application, 23-characters x 2-lines can be displayed, if the format of character font is 6 x 8 pixels.

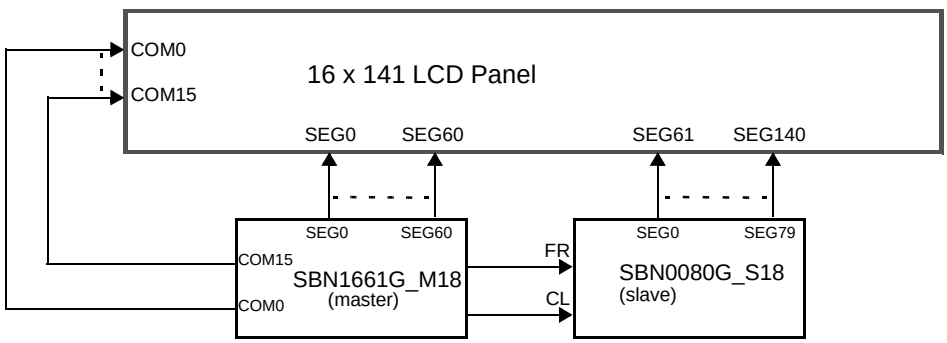
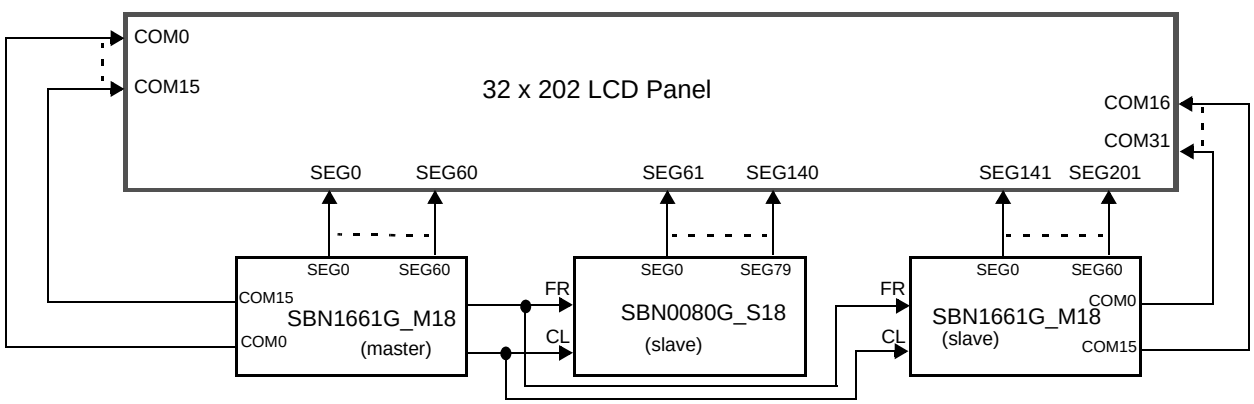



Fig.33 1/16 duty, 23 characters x 2 lines

### 17.3 1/32 duty, 33 characters x 4 lines

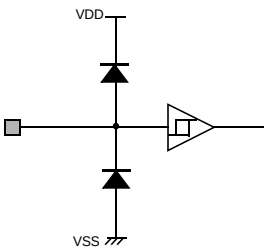
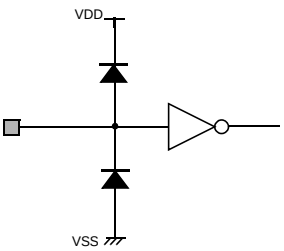
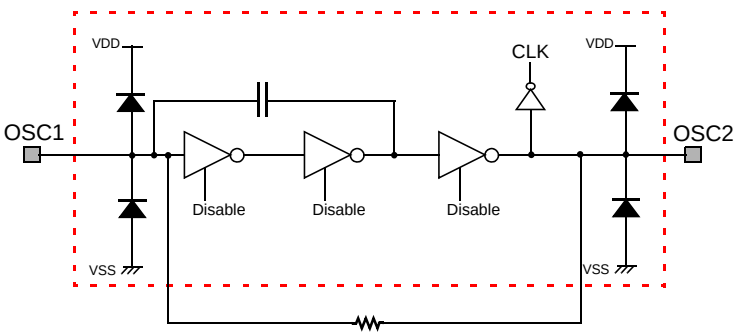
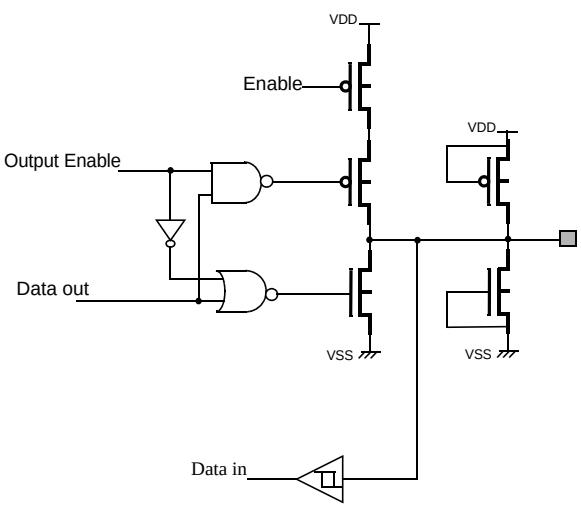


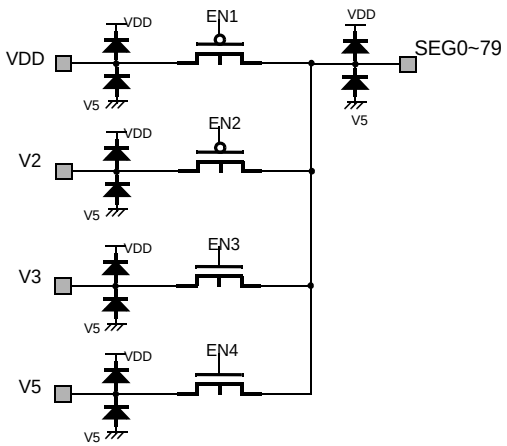
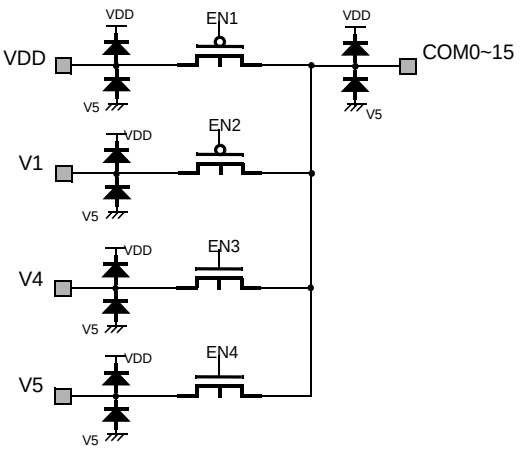

In this application, 33-characters x 4-lines can be displayed, if the format of character font is 6 x 8 pixels.

Fig.34 1/32 duty, 33 characters x 4 lines

## 18 PIN CIRCUITS

**Table 46** MOS-level schematics of all input, output, and I/O pins.

| SYMBOL | Input/ output | CIRCUIT | NOTES |
|---|---|---|---|
| $\overline{C}$/D, R/$\overline{W}$(WR), E/$\overline{RD}$, RESET/IF | Inputs |  | |
| M/$\overline{S}$ | Input |  | |
| OSC1, OSC2 | |  | The circuit encircled inside the red dashed frame is the oscillator circut. |
| D0~D7, FR | I/O |  | |

| SYMBOL | Input/ output | CIRCUIT | NOTES |
|---|---|---|---|
| SEG0~79 | |  | |
| COM0~15 | |  | |

## 19 APPLICATION NOTES

1. It is recommended that the following power-up sequence be followed to ensure reliable operation of your display system. As the ICs are fabricated in CMOS and there is intrinsic latch-up problem associated with any CMOS devices, proper power-up sequence can reduce the danger of triggering latch-up. When powering up the system, control logic power must be powered on first. When powering down the system, control logic must be shut off later than or at the same time with the LCD bias ($V_{EE}$).

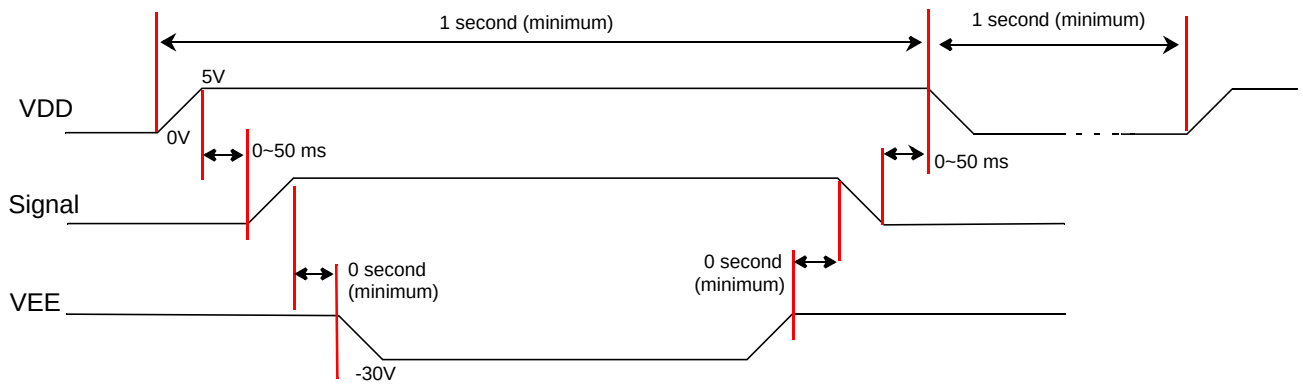



Fig.35 Recommended power up/down sequence

2. The metal frame of the LCD panel should be grounded.
3. A 0.1 μF ceramic capacitor should be connected between $V_{DD}$ and $V_{SS}$.
4. A 0.1 mF ceramic capacitor should be connected between $V_{DD}$ (or $V_{SS}$) and each of V1, V2, V3, V4, and V5.
5. If the length of the cable connecting the host microcontroller and the LCD module is longer than 45 cm, a ceramic capacitor of 20P~150P should be connected between $V_{DD}$ (or $V_{SS}$) and each of the R/$\overline{WR}$($\overline{WR}$), the E/$\overline{RD}$, and the $\overline{CS}$.

## 20 PACKAGE INFORMATION

Pakage information is provided in another document. Please contact Avant Electronics for package information.

# 21 SOLDERING

## 21.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. For more in-depth account of soldering ICs, please refer to dedicated reference materials.

## 21.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, please contact Avant for drypack information.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

## 21.3 Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

**If wave soldering cannot be avoided, the following conditions must be observed:**

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

## 21.4 Repairing soldered joints

Fix the component by first soldering two diagonally- opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## 22 LIFE SUPPORT APPLICATIONS

Avant's products, unless specifically specified, are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Avant customers using or selling Avant's products for use in such applications do so at their own risk and agree to fully indemnify Avant for any damages resulting from such improper use or sale.