ALL SHORE INDUSTRIES

ASI-O-293LAGGGF0/M

No.	Items	Specification	Unit
1	Display Mode	Passive Matrix OLED	-
2	Display Color	Monochrome (White)	-
3	Duty	1/16	-
4	Characters x lines	20 x 2	Pixel
5	Character Font	5 x 8	-
6	Active Area	73.52 (W) x 11.52 (H)	mm
7	Outline Dimension	84.50 (W) x 19.28 (H) x 2.00 (D)	mm
8	Character pitch	3.70 (W) x 5.95 (H)	mm
9	Character size	3.22 (W) x 5.57 (H)	mm
10	Pixel Pitch	0.65 (W) x 0.70 (H)	mm
11	Pixel Size	0.62 (W) x 0.67 (H)	mm
12	Driver IC	US2066	-
13	Interface	4-/8-bit parallel,SPI,I2C	-
14	Weight	7.01	g

REVISION RECORD

REV NO.	REV DATE	CONTENTS	REMARKS
1.0	2011-05-01	Preliminary	

CONTENT

■ PHYSICAL DATA

No.	Items	Specification	Unit
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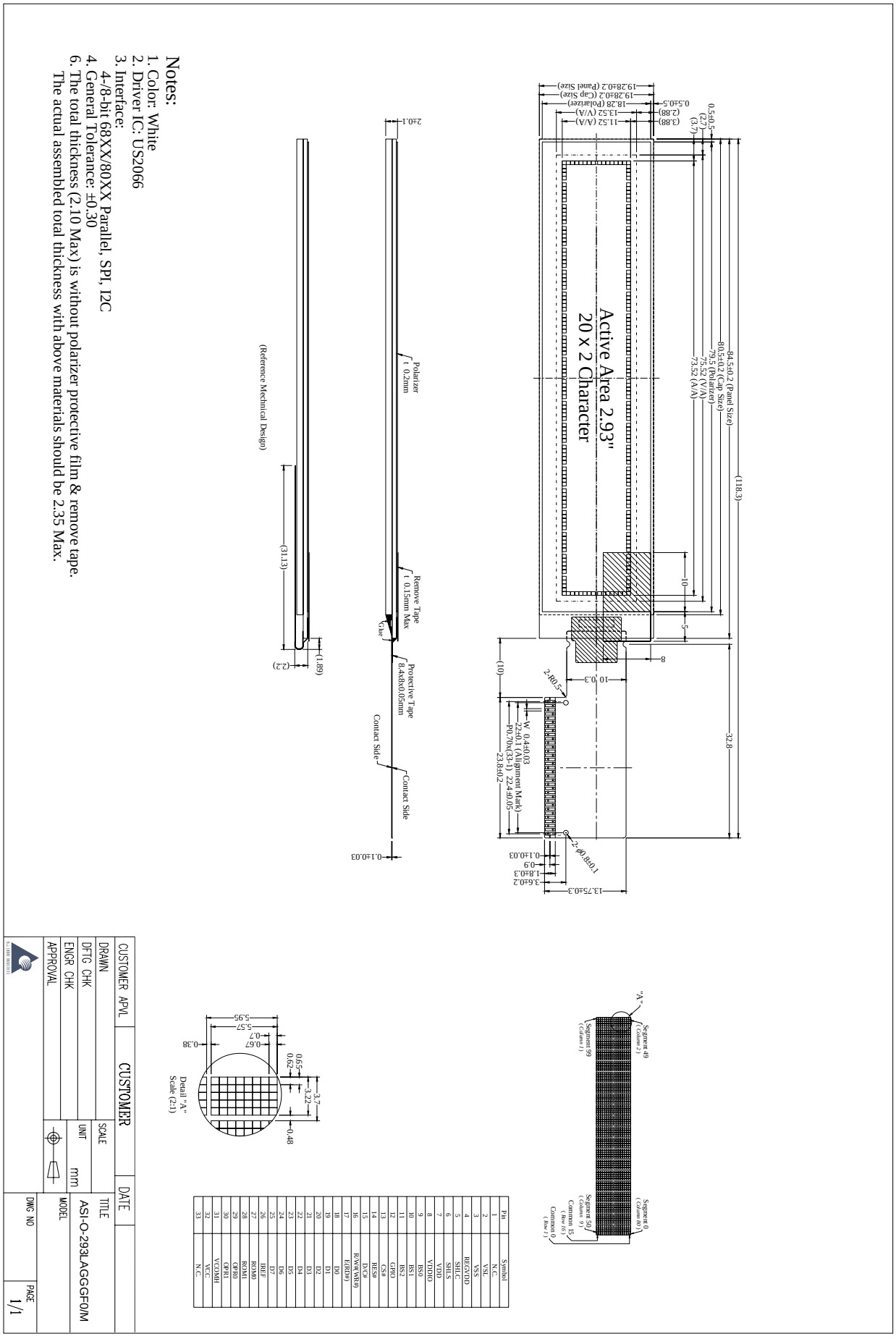
ALL SHORE INDUSTRIES

■ EXTERNAL DIMENSIONS



Pin	Symbol
1	N.C.
2	VSL
3	VSS
4	REGVDD
5	SHLC
6	SHLS
7	VDD
8	VDDIO
9	IBS0
10	IBS1
11	IBS2
12	GPIO
13	CS#
14	RES#
15	D/C#
16	R/W#(WR#)
17	E(RD#)
18	D0
19	D1
20	D2
21	D3
22	D4
23	D5
24	D6
25	D7
26	IREF
27	ROM0
28	ROM1
29	OPR0
30	OPR1
31	VCOMH
32	VCOM
33	N.C.

Notes:
1. Color: White
2. Driver IC: US2066
3. Interface:
   4-/8-bit 68XX/80XX Parallel, SPI, I2C
4. General Tolerance: ±0.30
6. The total thickness (2.10 Max) is without polarizer protective film & remove tape.
   The actual assembled total thickness with above materials should be 2.35 Max.

CUSTOMER APVL	CUSTOMER	DATE	
DRAWN			
DFTG CHK	SCALE	TITLE	ASI-O-293LAGGGF0/M
ENGR CHK	UNIT mm	MODEL	
APPROVAL		DWG NO	
		PAGE	1/1

■ ABSOLUTE MAXIMUM RATINGS

Items	Symbol	Min	Typ.	Max	Unit	Notes
Supply voltage for logic	V_{DD}	-0.3	-	6.0	V	1,2
Supply voltage for I/O pins	V_{DDIO}	-0.3	-	6.0	V	1,2
Supply voltage for display	V_{CC}	0	-	15.0	V	1,2
Operating temperature	T_{OP}	-40	-	85	℃	3
Storage temperature	T_{ST}	-40	-	90	℃	3
Life time(120cd/m^2)	-	30,000	-	-	hour	4
Humidity	-	-	-	90	%RH	-

Note 1: All the above voltages are on the basis of V_{SS} = 0V .

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur.Also,for normal operations,it is desirable to use this module under the conditions according to electro-optical characteristics .If this module is used beyond these conditions,malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature temperature of the polarizer should be 80°C.

Note 4: V_{CC} = 12.0V, T_a = 25°C, 50% Checkerboard.
Software configuration follows Actual Application Example .
End of lifetime is specified as 50% of initial brightness reached.The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

■ ELECTRICAL CHARACTERISTICS

DC Characteristics

Items	Symbol	Conditions	Min	Typ.	Max	Unit
Supply voltage for logic	V_{DD}	(Low voltage I/O application)	2.4	2.8	V_{DDIO}	V
Supply voltage for I/O pins	V_{DDIO}		2.4	2.8	3.6	V
Supply voltage for logic	V_{DD}	(5V I/O application)	-	-	-	V
Supply voltage for I/O pins	V_{DDIO}		4.4	5.0	5.5	V
Supply voltage for display	V_{CC}	Note 5	11.5	12	12.5	V
High level input	V_{IH}	I_{OUT} = 100μA, 3.3MH	0.8 x V_{DDIO}	-	V_{DDIO}	V
Low level input	V_{IL}	I_{OUT} = 100μA, 3.3MH	0	-	0.2x V_{DDIO}	V
High level output	V_{OH}	I_{OUT} = 100μA, 3.3MH	0.9 x V_{DDIO}	-	V_{DDIO}	V
Low level output	V_{OL}	I_{OUT} = 100μA, 3.3MH	0	-	0.1xV_{DDIO}	V
Operating current for V_{DD}	I_{DD}		-	180	300	μA
Operating current for V_{CC}	I_{CC}	Note 6	-	15.0	18.0	mA
		Note 7	-	23.7	28.6	mA
		Note 8	-	45.5	55.0	mA
Sleep mode current for V_{DD}	$I_{DD,SLEEP}$		-	1	10	μA
Sleep mode current for V_{CC}	$I_{CC,SLEEP}$		-	2	10	μA

Note 5: Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer s request.

Note 6: V_{DD} = 2.8V or 5.0V, V_{CC} = 12V, 30% Display Area Turn on.
Note 7: V_{DD} = 2.8V or 5.0V, V_{CC} = 12V, 50% Display Area Turn on.
Note 8: V_{DD} = 2.8V or 5.0V, V_{CC} = 12V, 100% Display Area Turn on.

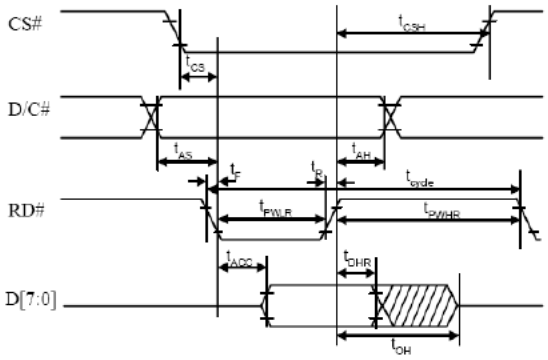
* Software configuration follows Actual Application Example .

◆AC Characteristics

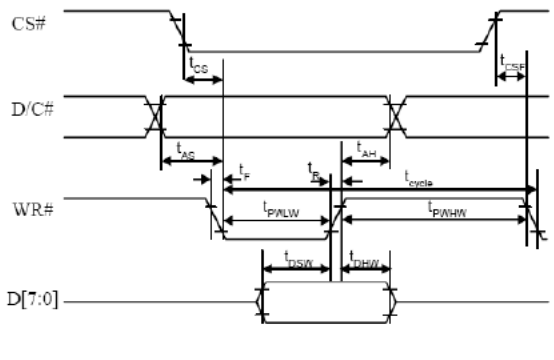
1. 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time (Write Cycle)	400	-	ns
t_{AS}	Address Setup Time	13	-	ns
t_{AH}	Address Hold Time	17	-	ns
t_{DSW}	Write Data Setup Time	35	-	ns
t_{DHW}	Write Data Hold Time	18	-	ns
t_{DHR}	Read Data Hold Time	13	-	ns
t_{OH}	Output Disable Time	10	70	ns
t_{ACC}	Access Time (RAM)	-	125	ns
	Access Time (Command)			
t_{CS}	Chip Select Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	0	-	ns
PW_{CSL}	Chip Select Low Pulse Width (Read RAM) - t_{PWLR}	250	-	ns
	Chip Select Low Pulse Width (Read Command) - t_{PWLR}	250		
	Chip Select Low Pulse width (Write) - t_{PWLW}	50		
PW_{CSH}	Chip Select High Pulse Width (Read) - t_{PWHR}	155	-	ns
	Chip Select High Pulse Width (Write) - t_{PWHW}	55		
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DDIO} - V_{SS} = 2.4V to 3.6V / 4.4V to 5.5V, T_a = 25°C)



(*Read Timing*)

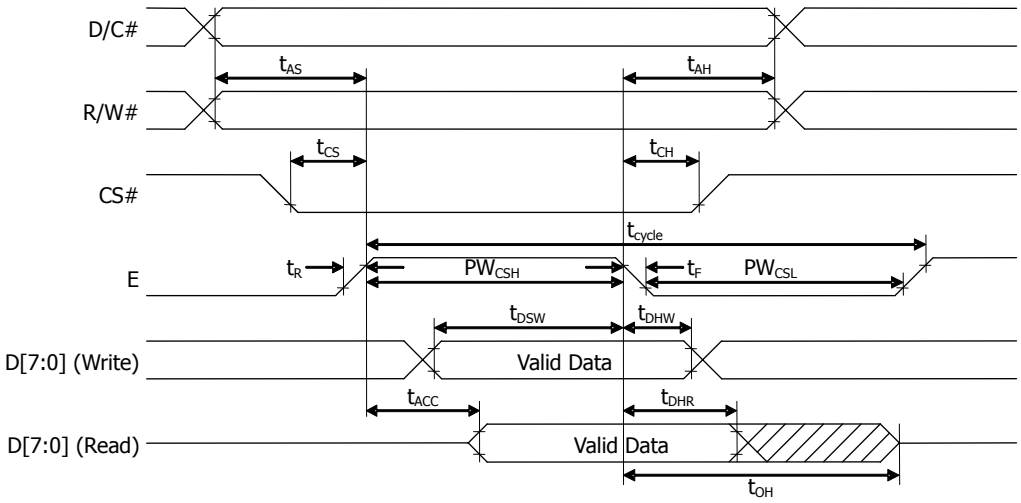


(*Write Timing*)

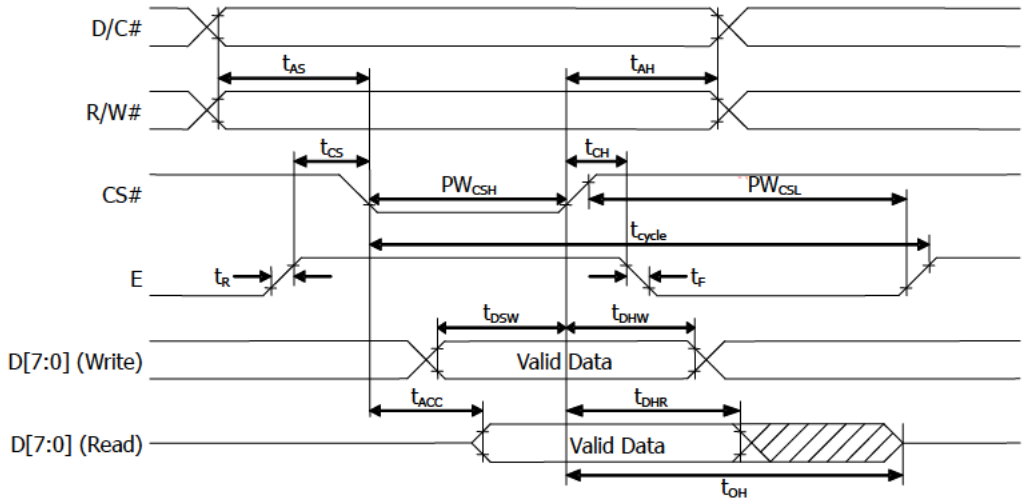
2. 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time (Write Cycle)	400	-	ns
t_{AS}	Address Setup Time	13	-	ns
t_{AH}	Address Hold Time	17	-	ns
t_{DSW}	Write Data Setup Time	35	-	ns
t_{DHW}	Write Data Hold Time	18	-	ns
t_{DHR}	Read Data Hold Time	13	-	ns
t_{OH}	Output Disable Time	10	90	ns
t_{ACC}	Access Time (RAM)	-	125	ns
	Access Time (Command)			
t_{CS}	Chip Select Time	0	-	ns
t_{CH}	Chip Select Hold Time	0	-	ns
PW_{CSL}	Chip Select Low Pulse Width (Read RAM)	250	-	ns
	Chip Select Low Pulse Width (Read Command)	250		
	Chip Select Low Pulse width (Write)	50		
PW_{CSH}	Chip Select High Pulse Width (Read)	155	-	ns
	Chip Select High Pulse Width (Write)	55		
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DDIO} - V_{SS} = 2.4V to 3.6V / 4.4V to 5.5V, T_a = 25°C)



(CS# "Low Pulse Width" > E "High Pulse Width")

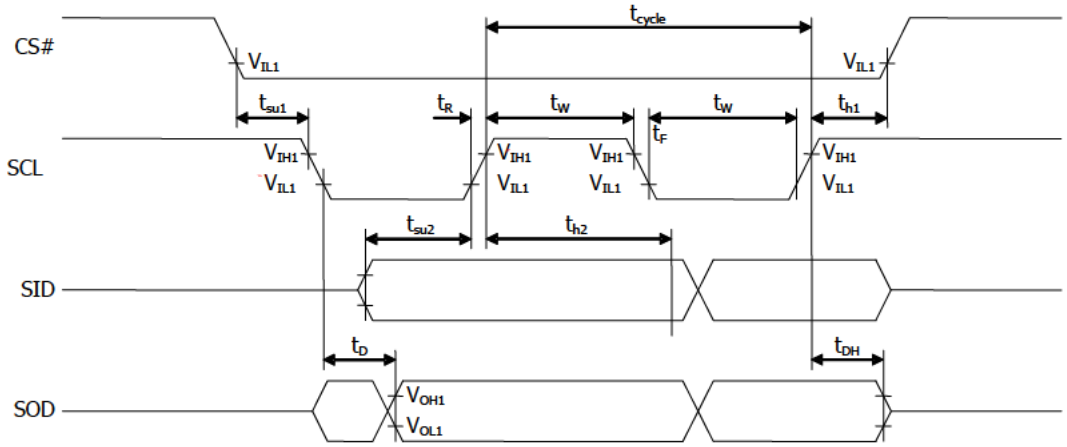


(CS# "Low Pulse Width" < E "High Pulse Width")

3. Serial Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Serial Clock Cycle Time	1	20	ns
t_{su1}	Chip Select Setup Time	60	-	ns
t_{h1}	Chip Select Hold Time	20	-	ns
t_{su2}	Serial Input Data Setup Time	200	-	ns
t_{h2}	Serial Input Data Hold Time	TBD	-	ns
t_D	Serial Output Data Delay Time	-	TBD	ns
t_{DH}	Serial Output Data Hold Time	10	-	ns
t_W	Serial Clock Width (Low, High)	400	-	ns
t_R	Serial Clock Rise Time	-	15	ns
t_F	Serial Clock Fall Time	-	15	ns

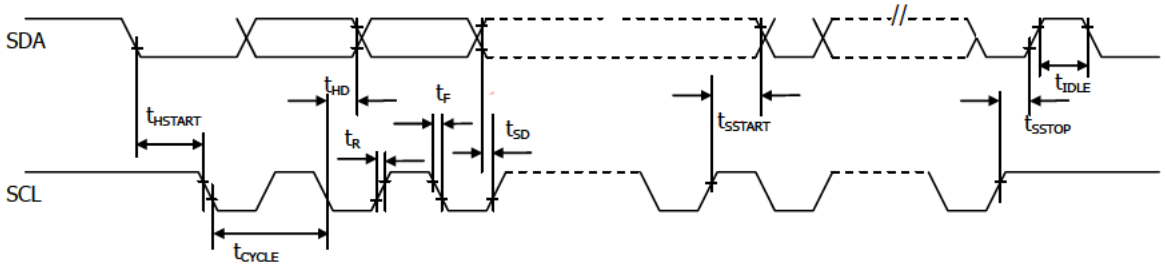
* (V_{DDIO} - V_{SS} = 2.4V to 3.6V / 4.4V to 5.5V, T_a = 25°C)



4. I²C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	µs
t_{HSTART}	Start Condition Hold Time	0.6	-	µs
t_{HD}	Data Hold Time (for "SDA_{OUT}" Pin)	5	-	ns
	Data Hold Time (for "SDA_{IN}" Pin)	300		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	µs
t_{SSTOP}	Stop Condition Setup Time	0.6	-	µs
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	µs

* (V_{DDIO} - V_{SS} = 2.4V to 3.6V / 4.4V to 5.5V, T_a = 25°C)



■ TIMING OF POWER SUPPLY

1. Commands

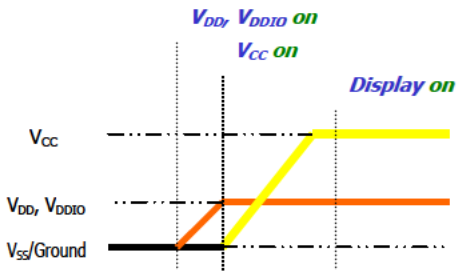
Refer to the Technical Manual for the US2066

2. Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

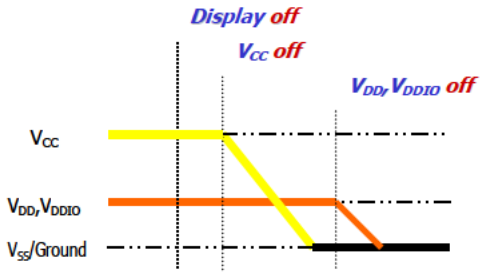
2.1 Power up Sequence:

1. Power up V_{DD} & V_{DDIO}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
   (When V_{CC} is stable)
7. Send Display on command



2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
   (When V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{DD} & V_{DDIO}



Note 9:

1) Since an ESD protection circuit is connected between V_{DD}, V_{DDIO} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} & V_{DDIO} whenever V_{DD} & V_{DDIO} is ON and V_{CC} is OFF.
2) V_{CC} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{DDIO}, V_{CC}) can never be pulled to ground under any circumstance.
4) V_{DD} & V_{DDIO} should not be power down before V_{CC} power down.

3. Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 5×8 Character Mode
3. Display start position is set at display RAM address 0
4. CGRAM address counter is set at 0
5. Cursor is OFF
6. Blink is OFF
7. Contrast control register is set at 7Fh
8. OLED command set is disabled

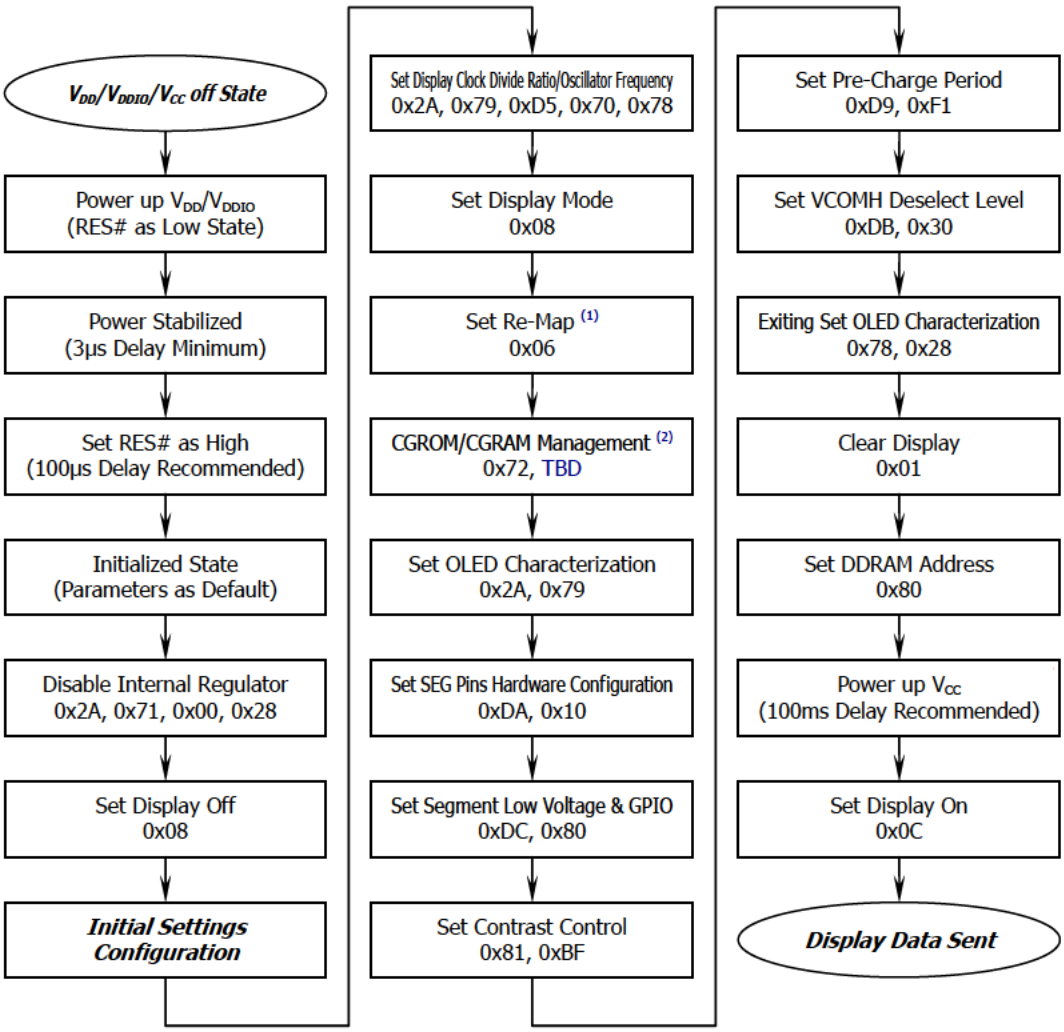
ASI-O-293LAGGGF0/M

4. Actual Application Example

Command usage and explanation of an actual example

4.1 Low Voltage I/O Application

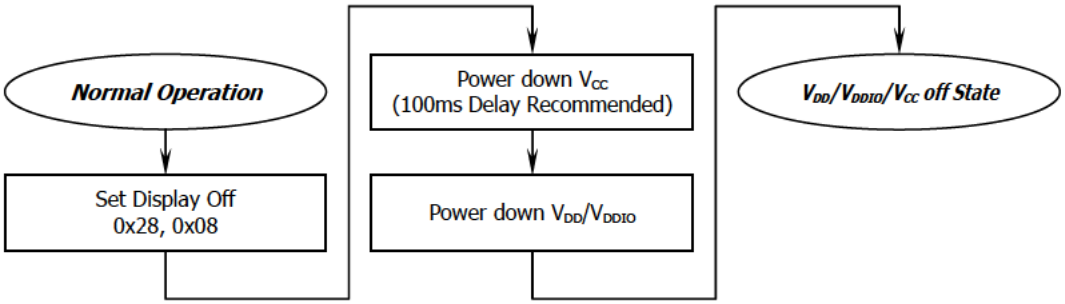
<Power up Sequence>



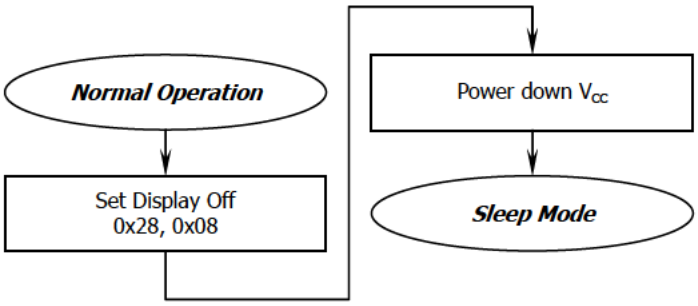
(1) This command could be programmable or defined by pin configuration.
(2) This command could be programmable or defined by pin configuration. The written value of the parameter should depend on the selection from Section 5 & 6

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

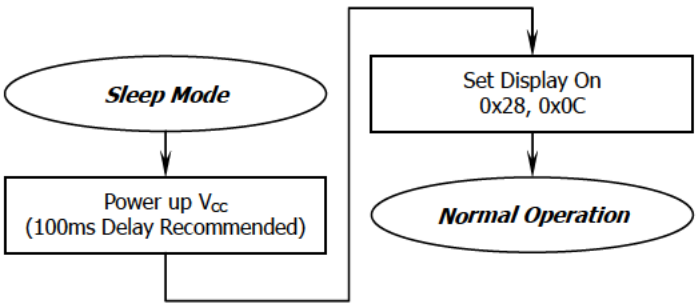
<Power down Sequence>



<Entering Sleep Mode>

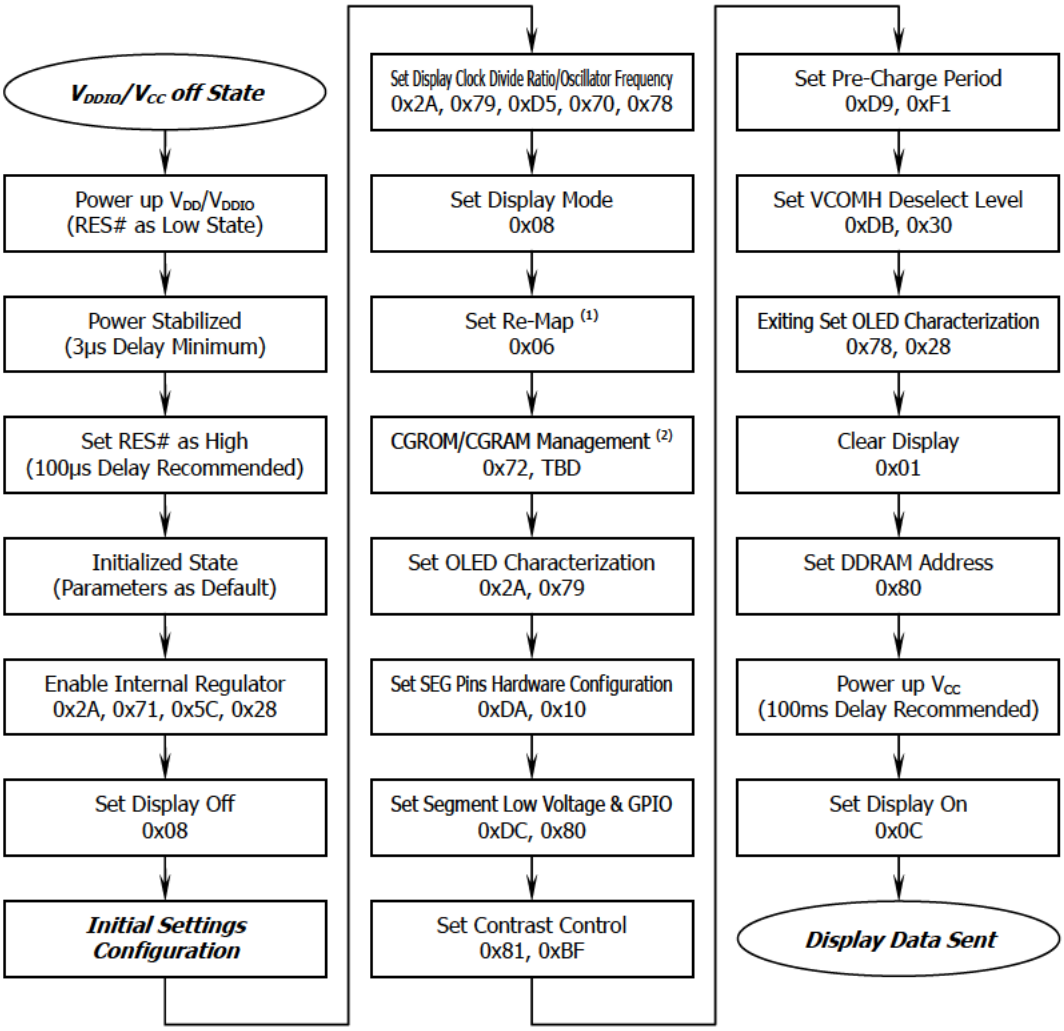


<Exiting Sleep Mode>



4.2 5V I/O Application

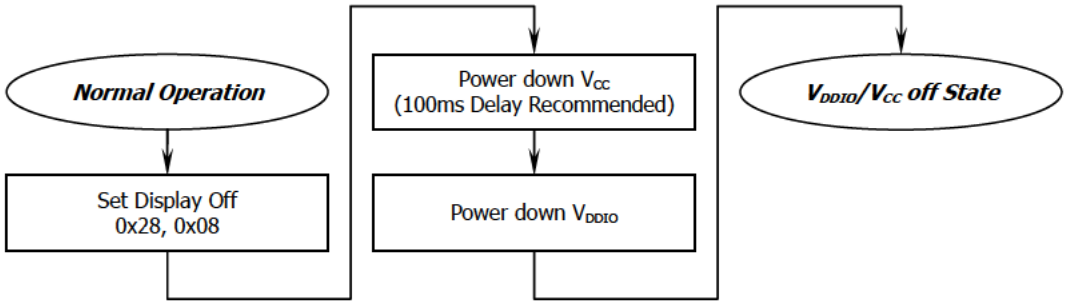
<Power up Sequence>



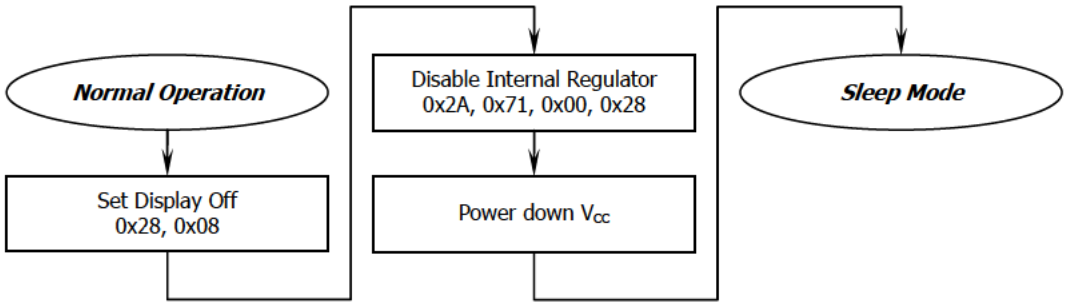
(1) This command could be programmable or defined by pin configuration.
(2) This command could be programmable or defined by pin configuration. The written value of the parameter should depend on the selection from Section 5 & 6

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

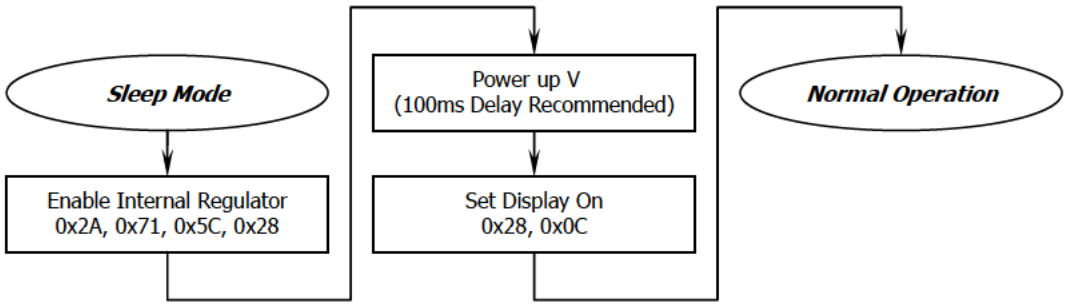
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>

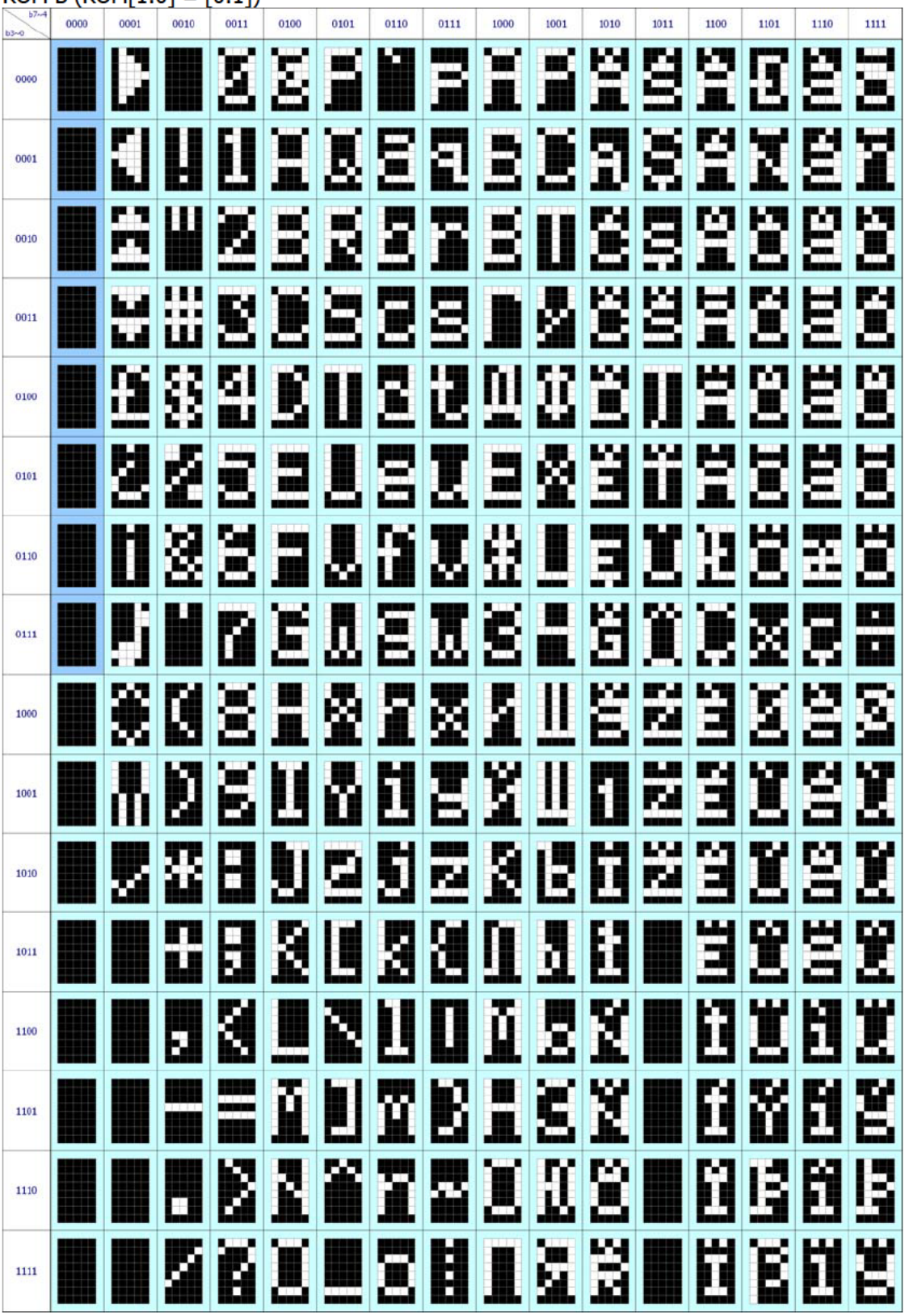


5. Built-in CGROM (Character Generator ROM)

ROM A (ROM[1:0] = [0:0])

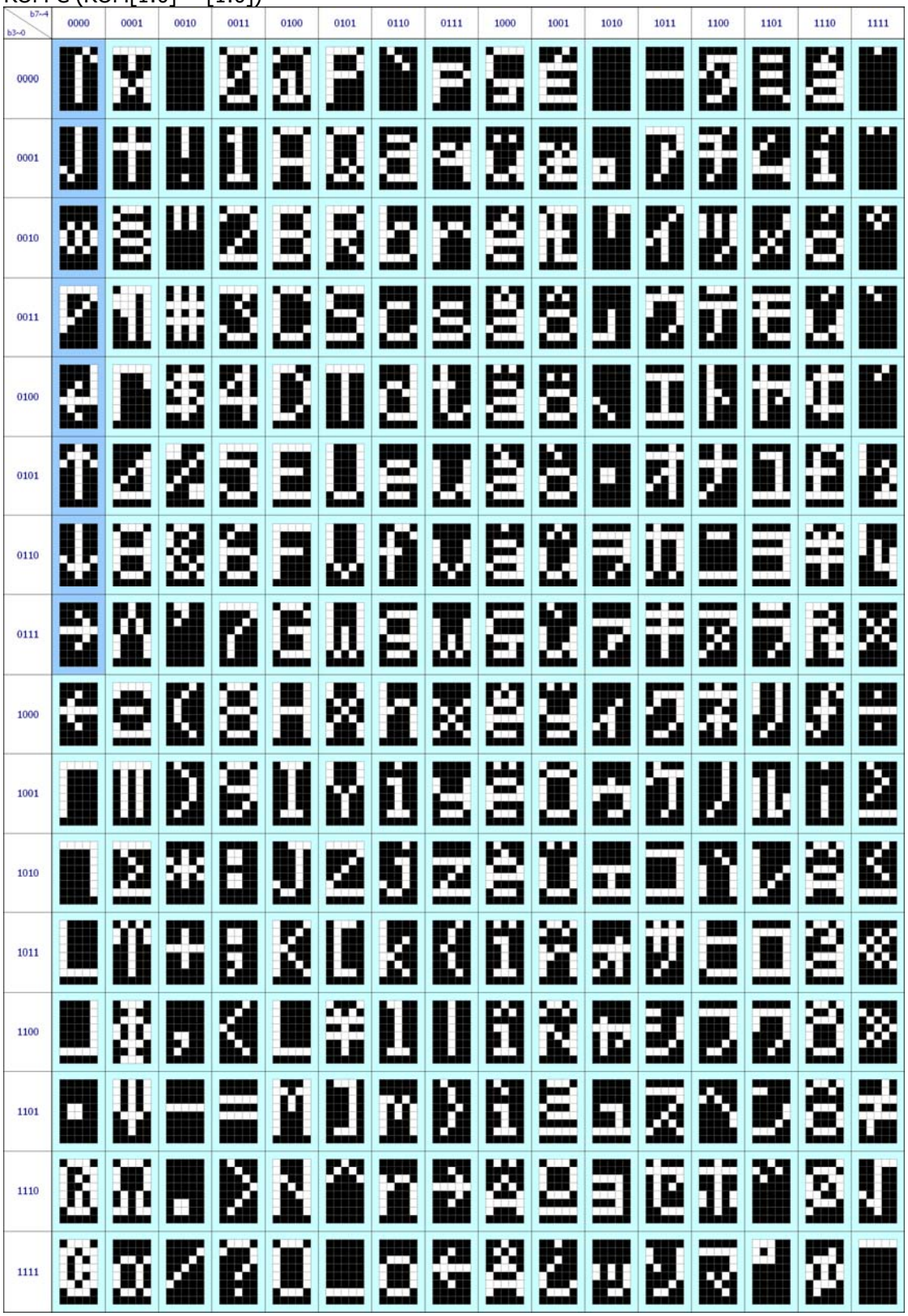
Language: English, Irish, Spanish, Dutch (2), Danish, Norwegian, Swedish, Finnish, Czech (7), Slovene, Hungarian (2), Turkish (1)
The number in the parentheses is showing how many letters might be needed to build and define additionally at CGRAM. The darker background is showing the maximum addresses (00h~07h) those could be allocated by OPR[1:0] setting.

ROM B (ROM[1:0] = [0:1])



Language: English, Irish, Portuguese, Spanish, French (1), Italian, German, Dutch (2), Icelandic, Danish, Norwegian, Swedish, Polish (8), Czech (8), Hungarian (2), Romanian (5), Turkish, Vietnamese (6), Russian (Small Letters)
The number in the parentheses is showing how many letters might be needed to build and define additionally at CGRAM. The darker background is showing the maximum addresses (00h~07h) those could be allocated by OPR[1:0] setting.

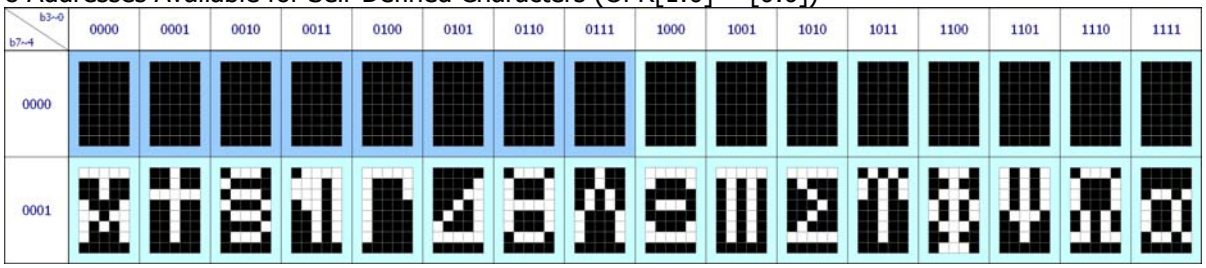
ROM C (ROM[1:0] = [1:0])



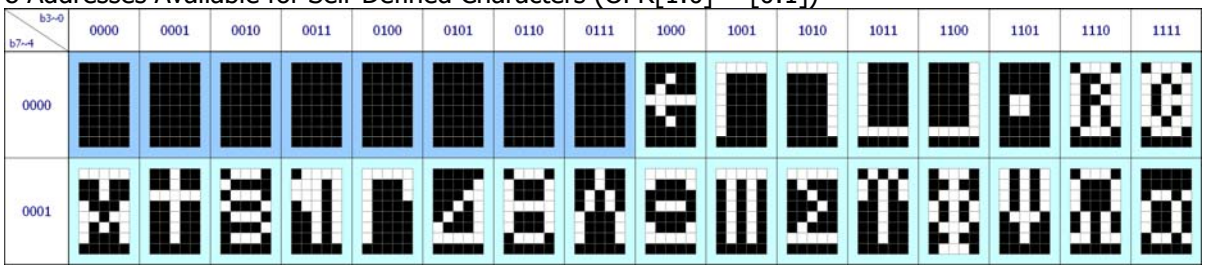
Language: English, Dutch (2), Japanese, Greek (Small Letters)
The number in the parentheses is showing how many letters might be needed to build and define additionally at CGRAM. The darker background is showing the maximum addresses (00h~07h) those could be allocated by OPR[1:0] setting.

6. Self-Defined CGRAM (Character Generator RAM)

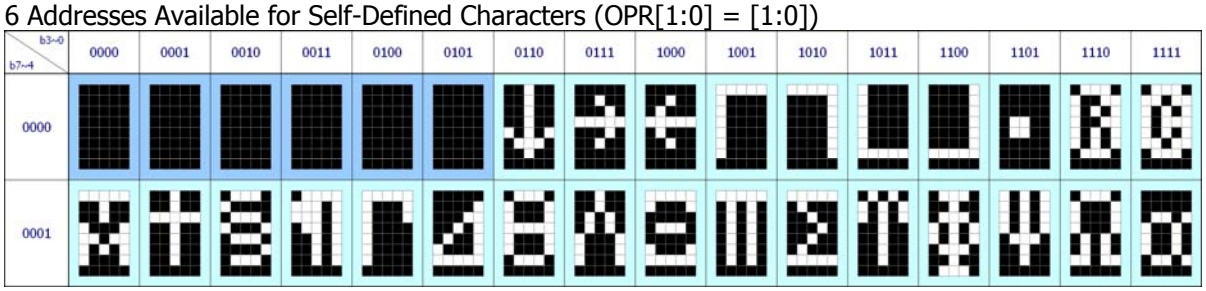
8 Addresses Available for Self-Defined Characters (OPR[1:0] = [0:0])



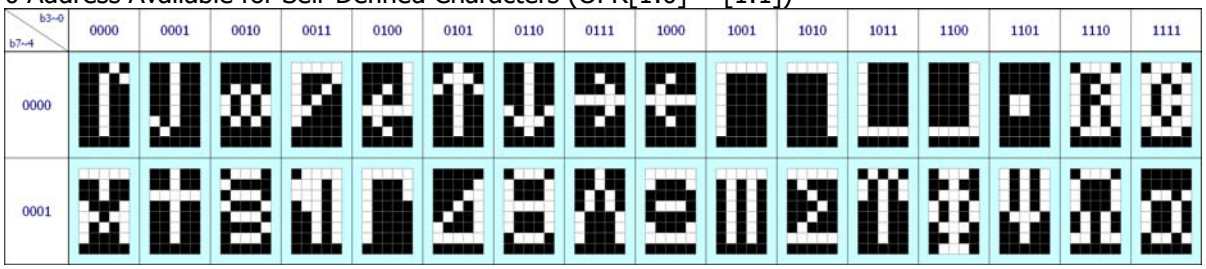
8 Addresses Available for Self-Defined Characters (OPR[1:0] = [0:1])



6 Addresses Available for Self-Defined Characters (OPR[1:0] = [1:0])



0 Address Available for Self-Defined Characters (OPR[1:0] = [1:1])



■ ELECTRO-OPTICAL CHARACTERISTICS (Ta=25℃)

Items		Symbol	Min.	Typ.	Max.	Unit	Remark
Operating Luminance		L	100	120	-	cd /m^2	White
Power Consumption		P	-	-	-	mW	30% pixels ON L=110cd/m^2
Frame Frequency		Fr	-	-	-	Hz	
Color Coordinate	White	CIE x	0.25	0.29	0.33	CIE1931	Darkroom
		CIE y	0.27	0.31	0.35		
Response Time	Rise	Tr	-	-	-	ms	-
	Decay	Td	-	-	-	ms	-
Contrast Ratio*		Cr	10000 :1	-	-		Darkroom
Viewing Angle Uniformity		△ θ	-	Free	-	Degree	-

Note : Brightness (L_{br}) is subject to the change of the panel characteristics and the customer s request.

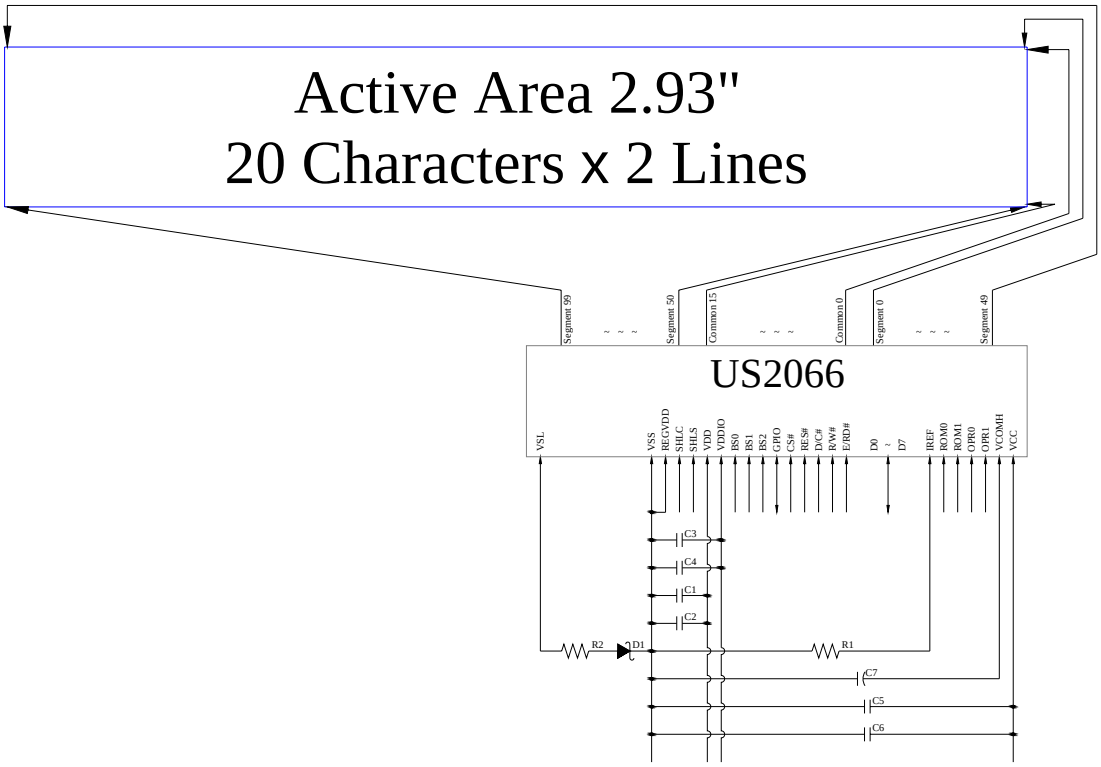
* Optical measurement taken at V_{DD} = 2.8V or 5.0V, V_{CC} = 12.0V.

Software configuration follows Actual Application Example .

■ INTERFACE PIN CONNECTIONS

1. Block Diagram

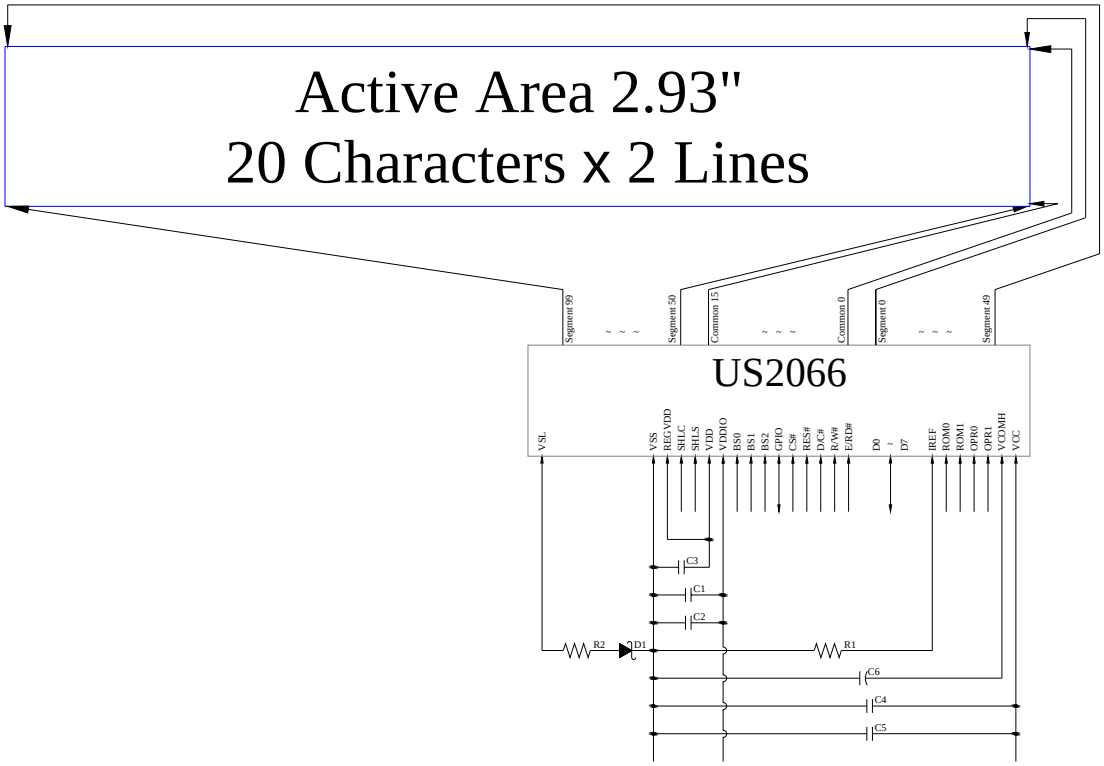
1.1 Low Voltage I/O Application



MCU Interface Selection: BS0, BS1 and BS2
Pins connected to MCU interface: CS#, RES#, D/C#, R/W#, E/RD#, and D0~D7
* SHLC, SHLC, ROM0, ROM1, OPR0 and OPR1 should be configured.

C1, C3, C5: 0.1μF
C2, C4: 4.7μF
C6: 10μF
C7: 4.7μF / 25V Tantalum Capacitor
R1: 470kΩ, R1 = (Voltage at IREF - VSS) / IREF
R2: 50Ω, 1/4W
D1: ≤1.4V, 0.5W

1.2 5V I/O Application



MCU Interface Selection: BS0, BS1 and BS2
Pins connected to MCU interface: CS#, RES#, D/C#, R/W#, E/RD#, and D0~D7
* SHLC, SHLC, ROM0, ROM1, OPR0 and OPR1 should be configured.

C1, C4: 0.1μF
C2: 4.7μF
C3: 1μF
C5: 10μF
C6: 4.7μF / 25V Tantalum Capacitor
R1: 470kΩ, R1 = (Voltage at IREF - VSS) / IREF
R2: 50Ω, 1/4W
D1: ≤1.4V, 0.5W

2. Pin Definition

Pin Number	Symbol	I/O	Function
Power Supply			
7	VDD	P	**Power Supply for Logic Circuit** This is a voltage supply pin which is supplied externally or regulated internally. A capacitor should be connected between this pin and V_{SS} under all circumstances. When internal V_{DD} is disabled, this is a power input pin. It must be connected to V_{DDIO} or external source and always be equal to or lower than V_{DDIO}. (Low Voltage I/O Application) When internal V_{DD} is enabled, it is regulated internally from V_{DDIO}. (*5V I/O Application*)
8	VDDIO	P	**Power Supply for Interface Logic Level** This is a voltage supply pin. It should match with the MCU interface voltage level and must be connected to external source
3	VSS	P	**Ground of OEL System** This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground.
32	VCC	P	**Power Supply for OEL Panel** This is the most positive voltage supply pin of the chip. It must be connected to external source.
Driver			
26	IREF	I	**Current Reference for Brightness Adjustment** This pin is segment current reference pin. A resistor should be connected between this pin and V_{SS}. Set the current at 15µA.
31	VCOMH	P	**Voltage Output High Level for COM Signal** This pin is the input pin for the voltage output high level for COM si nals. A capacitor should be connected between this pin and V_{SS}
2	VSL	P	**Voltage Output Low Level for SEG Signal** This is segment voltage reference pin. When external V_{SL} is not used, this pin should be left open. When external V_{SL} is used, this pin should connect with resistor and diode to ground.
External IC Communication			
12	GPIO	I/O	**General Purpose Input/Output** This pin could be left open individually or have signal inputted/outputted. It is able to use as the external DC/DC converter circuit enabled/disabled control or other applications.
Configuration			
4	REGVDD	I	**5V I/O Regulator Configuration** This is internal V_{DD} regulator selection pin in 5V I/O application mode. When this pin is pulled "Low", internal V_{DD} regulator is disabled. (Low Voltage I/O Application) When this pin is pulled "High", internal V_{DD} regulator is enabled. (*5V I/O Application*)
5	SHLC	I	**Scanning Direction for COM Signal** This pin is used to determine COM output scanning direction. It can still be programmable and defined by fundamental command.
6	SHLS	I	**Mapping Direction for SEG Signal** This pin is used to change the mapping between the display data column address and the segment driver. It can still be programmable and defined by fundamental command.
27 28	ROM0 ROM1	I	**Built-in Character ROM Selection** These pins are used to select the appropriate character ROM. See the following table & Section 4.5: ROM A (Page 19): ROM0 = 0, ROM1 = 0 ROM B (Page 20): ROM0 = 1, ROM1 = 0 ROM C (Page 21): ROM0 = 0, ROM1 = 1 Software Selectable: ROM0 = 1, ROM1 = 1 It can still be programmable and defined by extended command.

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td colspan="4">Configuration(Continued)</td></tr>
<tr><td>29
30</td><td>OPR0
OPR1</td><td>I</td><td>Character ROM/RAM Management
These pins are used to manage the character number of character generator. See the following table & Section 4.6:
<table>
<tr><th>CGROM</th><th>CGRAM</th><th>OPR0</th><th>OPR1</th></tr>
<tr><td>240</td><td>8</td><td>0</td><td>0</td></tr>
<tr><td>248</td><td>8</td><td>1</td><td>0</td></tr>
<tr><td>250</td><td>6</td><td>0</td><td>1</td></tr>
<tr><td>256</td><td>0</td><td>1</td><td>1</td></tr>
</table>
It can still be programmable and defined by extended command.</td></tr>
<tr><td colspan="4">Interface</td></tr>
<tr><td>9
10
11</td><td>BS0
BS1
BS2</td><td>I</td><td>Communicating Protocol Selection
These pins are MCU interface selection input. See the following table:
<table>
<tr><th></th><th>BS0</th><th>BS1</th><th>BS2</th></tr>
<tr><td>I²C</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>SPI</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>4-bit 68XX Parallel</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>4-bit 80XX Parallel</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>8-bit 68XX Parallel</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>8-bit 80XX Parallel</td><td>0</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>14</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset si nal input. When the pin is low, initialization of the chip is executed.</td></tr>
<tr><td>13</td><td>CS#</td><td>I</td><td>Chip Select
his pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>15</td><td>D/C#</td><td>I</td><td>Data/Command Control
This pin is Data/Command control pin. When the pin is pulled hi h, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
When the pin is pulled high and serial interface mode is selected, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I²C mode, this pin acts as SA0 for slave address selection.</td></tr>
<tr><td>17</td><td>E/RD#</td><td>I</td><td>Read/Write Enable or Read
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low.
When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.</td></tr>
<tr><td>16</td><td>R/W#</td><td>I</td><td>Read/Write Select or Write
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode.
When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.</td></tr>
<tr><td>18~25</td><td>D0~D7</td><td>I/O</td><td>Host Data Input/Output Bus
These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I²C mode is selected, D2, D1 should be tired together and serve as SDA_{OUT}, SDA_{IN} in application and D0 is the serial clock input, SCL.</td></tr>
<tr><td colspan="4">Reserve</td></tr>
<tr><td>1, 33</td><td>N.C. (GND)</td><td>-</td><td>Reserved Pin (Supporting Pin)
The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.</td></tr>
</table>

■ RELIABILITY TESTS

<table>
<tr><th colspan="2">Item</th><th>Condition</th><th>Criterion</th></tr>
<tr><td colspan="2">High Temperature Storage
(HTS)</td><td>90±2℃, 240 hours</td><td rowspan="6">1. After testing, the function test is ok.
2. After testing, no addition to the defect.
3. After testing, the change of luminance should be within +/- 50% of initial value.
4. After testing, the change for the mono and area color must be within (+/-0.02, +/- 0.02) and for the full color it must be within (+/-0.04, +/-0.04) of initial value based on 1931 CIE coordinates.
5. After testing, the change of total current consumption should be within +/- 50% of initial value.</td></tr>
<tr><td colspan="2">High Temperature Operating
(HTO)</td><td>85±2℃, 240 hours</td></tr>
<tr><td colspan="2">Low Temperature Storage
(LTS)</td><td>-40±2℃, 240 hours</td></tr>
<tr><td colspan="2">Low Temperature Operating
(LTO)</td><td>-40±2℃, 240 hours</td></tr>
<tr><td colspan="2">High Temperature / High Humidity Storage
(HTHHS)</td><td>60±3℃, 90%±3%RH, 240 hours</td></tr>
<tr><td colspan="2">Thermal Shock (Non-operation)
(TS)</td><td>-40±2℃ ~ 25℃ ~ 85±2℃
(30min) (5min) (30min)
100cycles</td></tr>
<tr><td>Vibration (Packing)</td><td>10~55~10Hz,amplitude 1.5mm, 1 hour for each direction x, y, z</td><td colspan="2" rowspan="2">1. One box for each test.
2. No addition to the cosmetic and the electrical defects.</td></tr>
<tr><td>Drop (Packing)</td><td>Height : 1 m, each time for 6 sides, 3 edges, 1 angle</td></tr>
</table>

Note： 1) For each reliability test, the sample quantity is 3, and only for one test item.
2) The HTHHS test is requested the Pure Water(Resistance＞10MΩ).

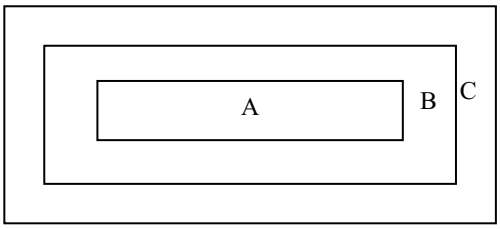
■OUTGOING QUALITY CONTROL SPECIFICATION

◆Standard

According to GB/T2828.1-2003/ISO 2859-1：1999 and ANSI/ASQC Z1.4-1993, General Inspection Level II.

◆Definition

1 Major defect : The defect that greatly affect the usability of product.
2 Minor defect : The other defects, such as cosmetic defects, etc.
3 Definition of inspection zone:



Zone A: Active Area

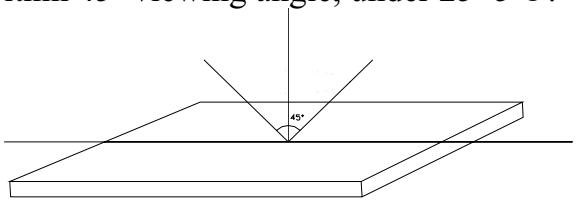
Zone B: Viewing Area except Zone A

Zone C: Outside Viewing Area

Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble of quality and assembly to customer`s product.

◆Inspection Methods

1 The general inspection : under 20W x 2 or 40W fluorescent light, about 30cm viewing distance, within 45º viewing angle, under 25±5℃.



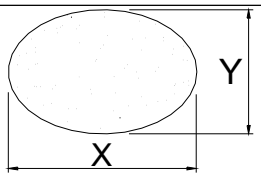
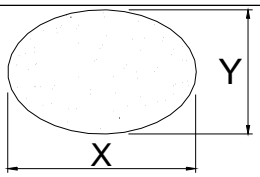
2 The luminance and color coordinate inspection : By PR705 or BM-7 or the equal equipments, in the dark room, under 25±5℃.

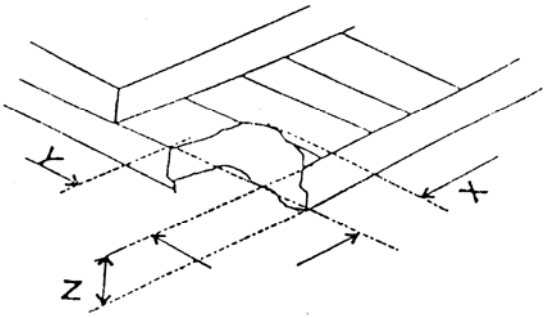
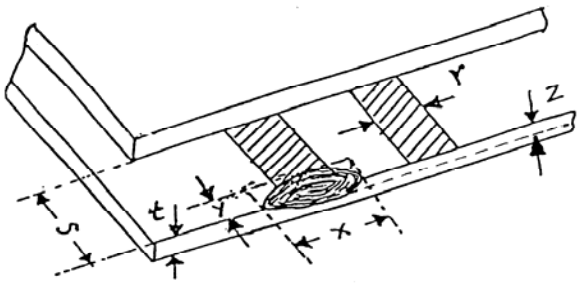
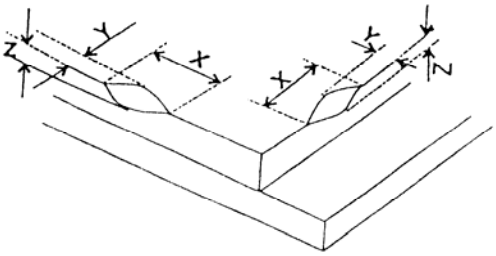
◆Inspection Criteria

1 Major defect : AQL= 0.65

Item	Criterion
Function Defect	1. No display or abnormal display is not accepted
	2. Open or short is not accepted.
	3. Power consumption exceeding the spec is not accepted.
Outline Dimension	Outline dimension exceeding the spec is not accepted.
Glass Crack	Glass crack tends to enlarge is not accepted.

2 Minor Defect : AQL= 1.5

<table>
<tr><td>Item</td><td colspan="4">Criterion</td></tr>
<tr><td rowspan="5">Spot Defect (dimming and lighting spot)</td><td colspan="2">Size (mm)</td><td colspan="2">Accepted Qty</td></tr>
<tr><td colspan="2"></td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="3">  </td><td>Φ≦0.10</td><td colspan="2">Ignored</td></tr>
<tr><td>0.10＜Φ≦0.15</td><td>3</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.15＜Φ≦0. 20</td><td>1</td></tr>
<tr><td colspan="4">Note : Φ= (x + y) / 2</td><td>0.20＜Φ</td><td>0</td></tr>
<tr><td rowspan="5">Line Defect (dimming and lighting line)</td><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.03</td><td colspan="2">Ignored</td></tr>
<tr><td>L≦3.0</td><td>0.03＜W≦0.05</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>L≦2.0</td><td>0.05＜W≦0.08</td><td>1</td></tr>
<tr><td>/</td><td>0.08＜W</td><td>As spot defect</td></tr>
<tr><td colspan="5">Remarks: The total of spot defect and line defect shall not exceed 4 pcs.</td></tr>
<tr><td>Polarizer Stain</td><td colspan="4">Stain which can be wiped off lightly with a soft cloth or similar cleaning is accepted, otherwise, according to the Spot Defect and the Line Defect.</td></tr>
<tr><td rowspan="7">Polarizer Scratch</td><td colspan="4">1. If scratch can be seen during operation, according to the criterions of the Spot Defect and the Line Defect.</td></tr>
<tr><td colspan="4">2. If scratch can be seen only under non-operation or some special angle, the criterion is as below :</td></tr>
<tr><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.03</td><td colspan="2">Ignore</td></tr>
<tr><td>5.0＜L≦10.0</td><td>0.03＜W≦0.05</td><td>2</td><td rowspan="3">Ignore</td></tr>
<tr><td>L≦5.0</td><td>0.05＜W≦0.08</td><td>1</td></tr>
<tr><td>/</td><td>0.08＜W</td><td>0</td></tr>
<tr><td rowspan="5">Polarizer Air Bubble</td><td colspan="2">Size</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="3">  </td><td>Φ≦0.20</td><td colspan="2">Ignored</td></tr>
<tr><td>0.20＜Φ≦0.50</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.50＜Φ≦0.80</td><td>1</td></tr>
<tr><td>0.80＜Φ</td><td>0</td></tr>
</table>

<table>
<tr><td rowspan="4">Glass Defect (Glass Chiped)</td><td>1. On the corner
 
(mm)
<table><tr><td>x</td><td>≤ 2.0</td></tr><tr><td>y</td><td>≤ S</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>2. On the bonding edge
 
(mm)
<table><tr><td>x</td><td>≤ a / 2</td></tr><tr><td>y</td><td>≤ s / 3</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>3. On the other edges
 
(mm)
<table><tr><td>x</td><td>≤ a / 5</td></tr><tr><td>y</td><td>≤ 1.0</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>Note: t: glass thickness ; s: pad width ; a: the length of the edge</td></tr>
<tr><td>TCP Defect</td><td>Crack, deep fold and deep pressure mark on the TCP are not accepted</td></tr>
<tr><td>Pixel Size</td><td>The tolerance of display pixel dimension should be within ±20% of the spec</td></tr>
<tr><td>Luminance</td><td>Refer to the spec or the reference sample</td></tr>
<tr><td>Color</td><td>Refer to the spec or the reference sample</td></tr>
</table>

■ CAUTIONS IN USING OLED MODULE

◆Precautions For Handling OLED Module:

1. OLED module consists of glass and polarizer. Pay attention to the following items when handling:
   i. Avoid drop from high, avoid excessive impact and pressure.
   ii. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead.
   iii. If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
   iv. Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
   v. Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
   vi. Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of iii.
2. Do not attempt to disassemble or process the OLED Module.
3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.
4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.
5. Be sure to keep the air pressure under 120 kPa, otherwise the glass cover is to be cracked.
6. Be careful to prevent damage by static electricity:
   i. Be sure to ground the body when handling the OLED Modules.
   ii. All machines and tools required for assembling, such as soldering irons, must be properly grounded.
   iii. Do not assemble and do no other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%-60% is recommended.
   iv. Peel off the protective film slowly to avoid the amount of static electricity generated.
   v. Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.
   vi. Be sure to use anti-static package.
7. Contamination on terminals can cause an electrochemical reaction and corrade the terminal circuit, so make it clean anytime.
8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.
9. When the logic circuit power is off, do not apply the input signals.
10. Power on sequence: $V_{DD} \rightarrow V_{PP}$, and power off sequence: $V_{PP} \rightarrow V_{DD}$.
11. Be sure to keep temperature, humidity and voltage within the ranges of the spec, otherwise shorten Module’ s life time, even make it damaged.
12. Be sure to drive the OLED Module following the Specification and Datasheet of IC controller, otherwise something wrong may be seen.

13. When displaying images, keep them rolling, and avoid one fixed image displaying more than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

◆Precautions For Soldering OLED Module:

1. Soldering temperature : 260°C ± 10°C.
2. Soldering time : 3-4 sec.
3. Repeating time : no more than 3 times.
4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

Precautions For Storing OLED Module:

1. Be sure to store the OLED Module in the vacuum bag with dessicant.
2. If the Module can not be used up in 1 month after the bag being opened, make sure to seal the Module in the vacuum bag with dessicant again.
3. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
4. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
5. It is recommended to keep the temperature between 0°C and 30°C , the relative humidity not over 60%.

Limited Warranty

Unless relevant quality agreements signed with customer and law enforcement, for a period of 12 months from date of production, all products (except automotive products) All Shore will replace or repair any of its OLED modules which are found to be functional defect when inspected in accordance with All Shore OLED acceptance standards (copies available upon request). Cosmetic/visual defects must be returned to All Shore within 90 days of shipment. Confirmation of such date should be based on freight documents. The warranty liability of All Shore is limited to repair and/or replacement on the terms above. All Shore will not be responsible for any subsequent or consequential events.

◆Return OLED Module Under Warranty:

1. No warranty in the case that the precautions are disregarded.
2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects.