



## ASI-O-110EAWWH40/M

No.	Items	Specification	Unit
1	Display Mode	Passive Matrix OLED	-
2	Display Color	Monochrome (White)	-
3	Duty	1/36	-
4	Resolution	128(H) x 36 (V)	Pixel
5	Active Area	26.86 (W) x 7.54 (H)	mm <sup>2</sup>
6	Outline Dimension	31.00 (W) x 14.30 (H) x 1.00 (D)	mm <sup>3</sup>
7	Dot Pitch	0.21 (W) x 0.21 (H)	mm <sup>2</sup>
8	Dot Size	0.19 (W) x 0.19 (H)	mm <sup>2</sup>
9	Aperture Rate	82	%
10	Driver IC	SH1106G	-
11	Interface	8-bit 6800,8-bit 8080,I2C,4-wire SPI	-
12	Weight	0.96±10%	g



**REVISION RECORD**

REV NO.	REV DATE	CONTENTS	REMARKS
1.0	2013-06-08	Initial Release	
2.0	2014-06-03	Old part # ASI-O-11012836-OO-QWS/M	



# CONTENT

- PHYSICAL DATA
- EXTERNAL DIMENSIONS
- ABSOLUTE MAXIMUM RATINGS
- ELECTRICAL CHARACTERISTICS
- FUNCTIONAL SPECIFICATION AND APPLICATION CIRCUIT
- ELECTRO-OPTICAL CHARACTERISTICS
- INTERFACE PIN CONNECTIONS
- RELIABILITY TESTS
- OUTGOING QUALITY CONTROL SPECIFICATION
- CAUTIONS IN USING OLED MODULE

■ **PHYSICAL DATA**

<b>No.</b>	<b>Items</b>	<b>Specification</b>	<b>Unit</b>
1	Display Mode	Passive Matrix OLED	-
2	Display Color	Monochrome (White)	-
3	Duty	1/36	-
4	Resolution	128(H) x 36(V)	Pixel
5	Active Area	26.86 (W) x 7.54 (H)	mm <sup>2</sup>
6	Outline Dimension	31.00 (W) x 14.30 (H) x 1.00 (D)	mm <sup>3</sup>
7	Dot Pitch	0.21 (W) x 0.21 (H)	mm <sup>2</sup>
8	Dot Size	0.19 (W) x 0.19 (H)	mm <sup>2</sup>
9	Aperture Rate	82	%
10	Driver IC	SH1106G	-
11	Interface	8-bit 6800,8-bit 8080,I2C,4-wire SPI	-
12	Weight	0.96± 10%	g

# EXTERNAL DIMENSIONS

**Specification:**

1. Display: OLED (White)
2. Format: 128\*36
3. Driver IC: SH11066
4. DUTY: 1/36
5. Operate Temp: -40° C ~ 70° C
6. Storage Temp: -40° C ~ 85° C
7. ROHS Compliant

**Dots: 128x36  
1.1'**

**Com & Seg Layout**

**Detail 1 "A" (20-1)**

Pin Assignment	NO.	SYMBOL
NC	1	NC
VCOMH	2	VCOMH
VPP	3	VPP
IRRF	4	IRRF
VDD2	5	VDD2
C1N	6	C1N
C1P	7	C1P
C2P	8	C2P
C2N	9	C2N
VSS	10	VSS
VBRFF (NC)	11	VBRFF (NC)
VDD1	12	VDD1
IM1	13	IM1
IM2	14	IM2
/CS	15	/CS
/RES	16	/RES
A0	17	A0
/WR	18	/WR
/RD	19	/RD
D0	20	D0
D1	21	D1
D2	22	D2
D3	23	D3
D4	24	D4
D5	25	D5
D6	26	D6
D7	27	D7
NC	28	NC

CUSTOMER APVL	DATE
DRAWN	SCALE
DFTG CHK	UNIT
ENGR CHK	MM
APPROVAL	MODEL
DWG NO	PAGE
	1/1

## ■ ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	MIN	MAX	UNIT	REMARK
Logic supply voltage	VDD1	-0.3	3.6	V	IC maximum rating
Charge pump regulator supply voltage	VDD2	-0.3	4.3	V	IC maximum rating
OLED operating voltage	VPP	-0.3	14.5	V	IC maximum rating
Operating Temp.	Top	-40	70	°C	-
Storage Temp	Tstg	-40	85	°C	-
Operation life time(360cd/m <sup>2</sup> )	-	10,000	-	Hrs	-

Note 1: All the above voltages are on the basis of "V<sub>SS</sub> = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to electro-optical characteristics. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: V<sub>PP</sub> = 9.0V, T<sub>a</sub> = 25°C, 50% Checkerboard.

Software configuration follows Actual Application Example.

End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

## ■ ELECTRICAL CHARACTERISTICS

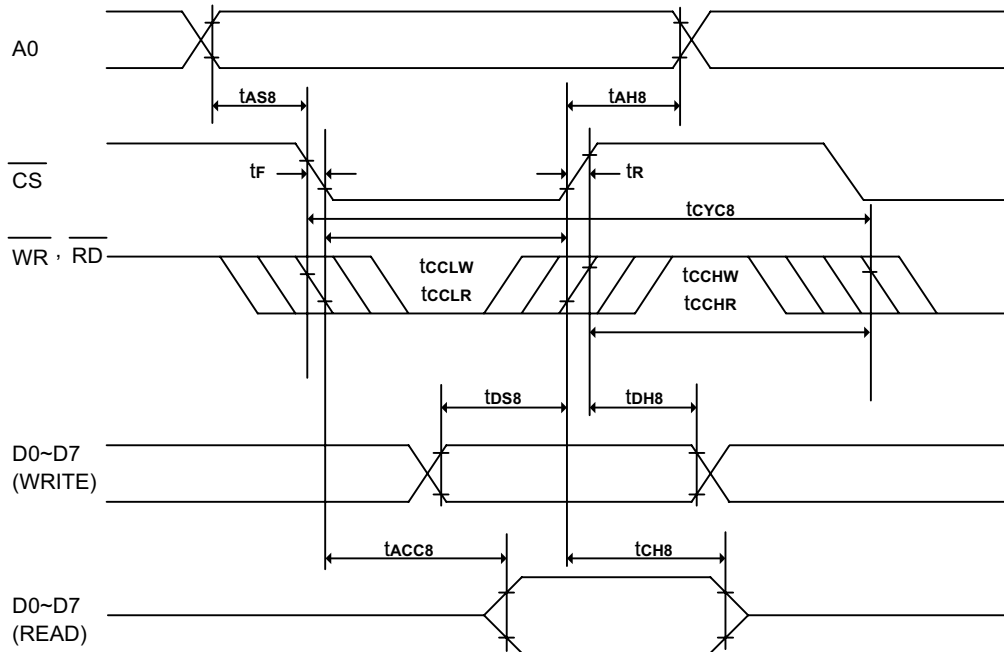
### ◆ DC Characteristics

ITEM	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Logic Supply Voltage	VDD1	22±3°C, 55±15%R.H	1.65	3.0	3.5	V
OLED Driver Supply Voltage (Generated by Internal DC/DC)	VPP	22±3°C, 55±15%R.H	-	9.0	-	V
Charge Pump Regulator Supply Voltage	VDD2	22±3°C, 55±15%R.H	3.0	3.7	4.2	V
High-level Input Voltage	V <sub>IH</sub>	-	0.8×VDD1	-	VDD1	V
Low-level Input Voltage	V <sub>IL</sub>	-	VSS	-	0.2×VDD1	V
High-level Output Voltage	V <sub>OH</sub>	-	0.8×VDD1	-	VDD1	V
Low-level Output Voltage	V <sub>OL</sub>	-	VSS	-	0.2×VDD1	V

Note : The VPP input must be kept in a stable value; ripple and noise are not allowed.

## ◆ AC Characteristics

### (1) System buses Read/Write characteristics 1 (For the 8080 Series Interface MPU)



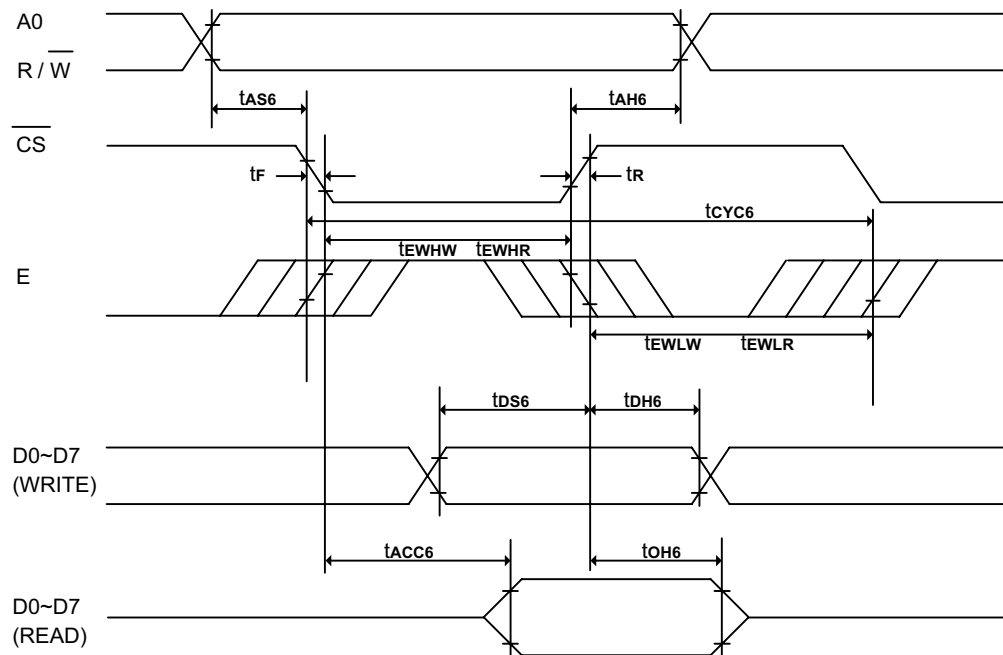
(VDD1 1.65 - 3.5V, TA +25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
t <sub>CYC8</sub>	System cycle time	600	-	-	ns	
t <sub>AS8</sub>	Address setup time	0	-	-	ns	
t <sub>AH8</sub>	Address hold time	0	-	-	ns	
t <sub>DS8</sub>	Data setup time	80	-	-	ns	
t <sub>DH8</sub>	Data hold time	30	-	-	ns	
t <sub>CH8</sub>	Output disable time	20	-	140	ns	C <sub>L</sub> 100pF
t <sub>ACC8</sub>	$\overline{RD}$ access time	-	-	280	ns	C <sub>L</sub> 100pF
t <sub>CCLW</sub>	Control L pulse width (WR)	200	-	-	ns	
t <sub>CCLR</sub>	Control L pulse width (RD)	240	-	-	ns	
t <sub>CCHW</sub>	Control H pulse width (WR)	200	-	-	ns	
t <sub>CCHR</sub>	Control H pulse width (RD)	200	-	-	ns	
t <sub>R</sub>	Rise time	-	-	30	ns	
t <sub>F</sub>	Fall time	-	-	30	ns	

(VDD1 2.4 - 3.5V, T<sub>A</sub> +25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
t <sub>CYC8</sub>	System cycle time	300	-	-	ns	
t <sub>AS8</sub>	Address setup time	0	-	-	ns	
t <sub>AH8</sub>	Address hold time	0	-	-	ns	
t <sub>DS8</sub>	Data setup time	40	-	-	ns	
t <sub>DH8</sub>	Data hold time	15	-	-	ns	
t <sub>CH8</sub>	Output disable time	10	-	70	ns	C <sub>L</sub> 100pF
t <sub>ACC8</sub>	$\overline{RD}$ access time	-	-	140	ns	C <sub>L</sub> 100pF
t <sub>CCLW</sub>	Control L pulse width (WR)	100	-	-	ns	
t <sub>CCLR</sub>	Control L pulse width (RD)	120	-	-	ns	
t <sub>CCHW</sub>	Control H pulse width (WR)	100	-	-	ns	
t <sub>CCHR</sub>	Control H pulse width (RD)	100	-	-	ns	
t <sub>R</sub>	Rise time	-	-	15	ns	
t <sub>F</sub>	Fall time	-	-	15	ns	

## (2) System buses Read/Write Characteristics 2 (For the 6800 Series Interface MPU)





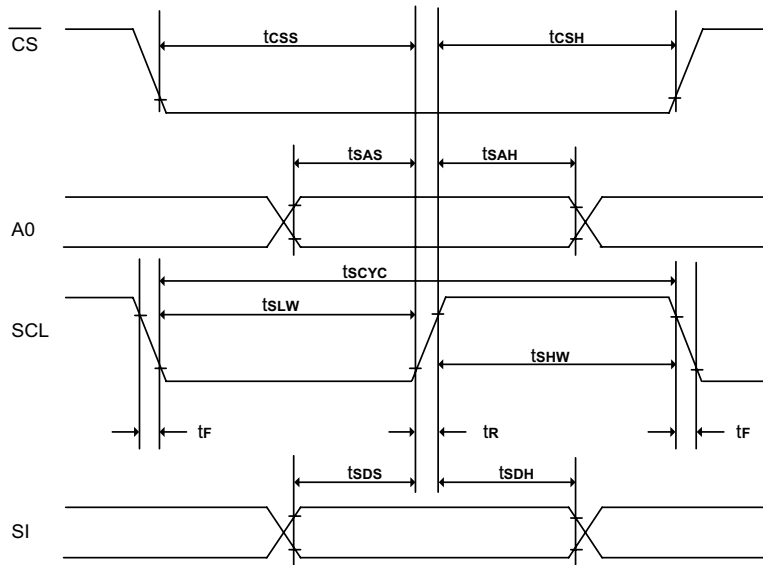
(VDD1 1.65 - 3.5V, TA +25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
t <sub>CYC6</sub>	System cycle time	600	-	-	ns	
t <sub>AS6</sub>	Address setup time	0	-	-	ns	
t <sub>AH6</sub>	Address hold time	0	-	-	ns	
t <sub>DS6</sub>	Data setup time	80	-	-	ns	
t <sub>DH6</sub>	Data hold time	30	-	-	ns	
t <sub>OH6</sub>	Output disable time	20	-	140	ns	C <sub>L</sub> 100pF
t <sub>ACC6</sub>	Access time	-	-	280	ns	C <sub>L</sub> 100pF
t <sub>EWHW</sub>	Enable H pulse width (Write)	200	-	-	ns	
t <sub>EWHR</sub>	Enable H pulse width (Read)	240	-	-	ns	
t <sub>EWLW</sub>	Enable L pulse width (Write)	200	-	-	ns	
t <sub>EWLR</sub>	Enable L pulse width (Read)	200	-	-	ns	
t <sub>R</sub>	Rise time	-	-	30	ns	
t <sub>F</sub>	Fall time	-	-	30	ns	

(VDD1 2.4 - 3.5V, TA +25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
t <sub>CYC6</sub>	System cycle time	300	-	-	ns	
t <sub>AS6</sub>	Address setup time	0	-	-	ns	
t <sub>AH6</sub>	Address hold time	0	-	-	ns	
t <sub>DS6</sub>	Data setup time	40	-	-	ns	
t <sub>DH6</sub>	Data hold time	15	-	-	ns	
t <sub>OH6</sub>	Output disable time	10	-	70	ns	C <sub>L</sub> 100pF
t <sub>ACC6</sub>	Access time	-	-	140	ns	C <sub>L</sub> 100pF
t <sub>EWHW</sub>	Enable H pulse width (Write)	100	-	-	ns	
t <sub>EWHR</sub>	Enable H pulse width (Read)	120	-	-	ns	
t <sub>EWLW</sub>	Enable L pulse width (Write)	100	-	-	ns	
t <sub>EWLR</sub>	Enable L pulse width (Read)	100	-	-	ns	
t <sub>R</sub>	Rise time	-	-	15	ns	
t <sub>F</sub>	Fall time	-	-	15	ns	

### (3) System buses Write characteristics 3(For the Serial Interface MPU)



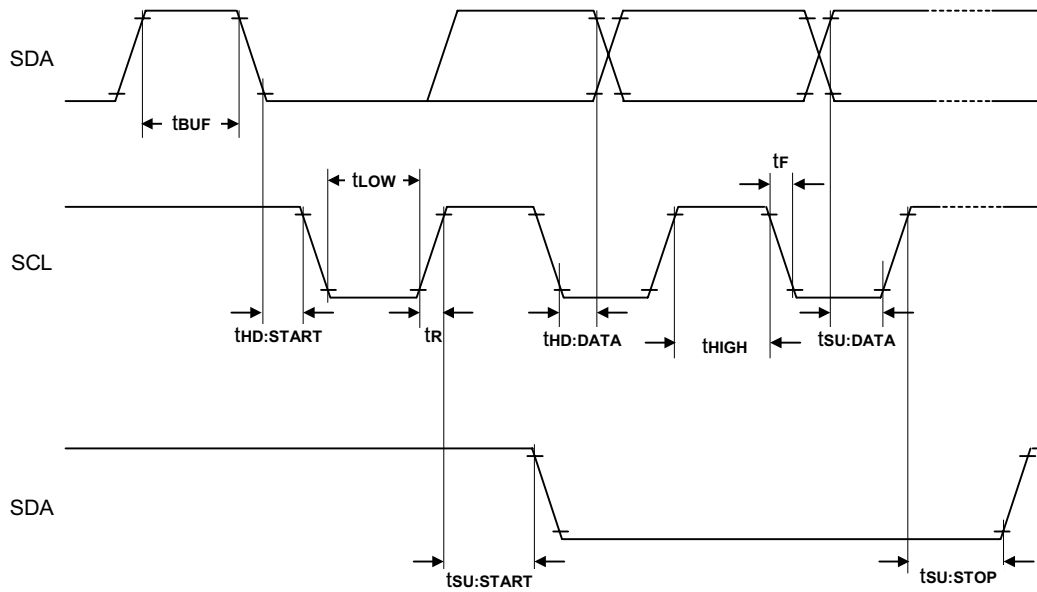
(VDD1 1.65 - 3.5V, T<sub>A</sub> +25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
tscYC	Serial clock cycle	500	-	-	ns	
tsAS	Address setup time	300	-	-	ns	
tsAH	Address hold time	300	-	-	ns	
tsDS	Data setup time	200	-	-	ns	
tsDH	Data hold time	200	-	-	ns	
tcSS	$\overline{CS}$ setup time	240	-	-	ns	
tcSH	$\overline{CS}$ hold time time	120	-	-	ns	
tshW	Serial clock H pulse width	200	-	-	ns	
tslW	Serial clock L pulse width	200	-	-	ns	
tr	Rise time	-	-	30	ns	
tf	Fall time	-	-	30	ns	

(VDD1 2.4 - 3.5V, T<sub>A</sub> +25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
tscYC	Serial clock cycle	250	-	-	ns	
tsAS	Address setup time	150	-	-	ns	
tsAH	Address hold time	150	-	-	ns	
tsDS	Data setup time	100	-	-	ns	
tsDH	Data hold time	100	-	-	ns	
tcSS	$\overline{CS}$ setup time	120	-	-	ns	
tcSH	$\overline{CS}$ hold time time	60	-	-	ns	
tshW	Serial clock H pulse	100	-	-	ns	
tslW	Serial clock L pulse	100	-	-	ns	
tr	Rise time	-	-	15	ns	
tf	Fall time	-	-	15	ns	

## (4) I<sup>2</sup>C interface characteristics

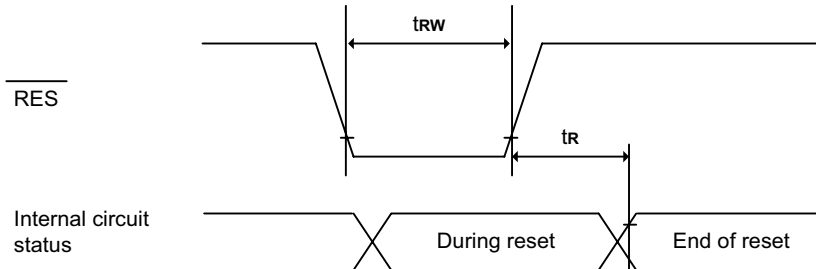


(VDD1 1.65 - 3.5V, TA +25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
$f_{SCL}$	SCL clock frequency	DC	-	400	kHz	
$T_{LOW}$	SCL clock Low pulse width	1.3	-	-	uS	
$T_{HIGH}$	SCL clock H pulse width	0.6	-	-	uS	
$T_{SU:DATA}$	data setup time	100	-	-	nS	
$T_{HD:DATA}$	data hold time	0	-	0.9	uS	
$T_R$	SCL , SDA rise time	$20+0.1C_b$	-	300	nS	
$T_F$	SCL , SDA fall time	$20+0.1C_b$	-	300	nS	
$C_b$	Capacity load on each bus line	-	-	400	pF	
$T_{SU:START}$	Setup time for re-START	0.6	-	-	uS	
$T_{HD:START}$	START Hold time	0.6	-	-	uS	
$T_{SU:STOP}$	Setup time for STOP	0.6	-	-	uS	
$T_{BUF}$	Bus free times between STOP and START condition	1.3	-	-	uS	

## ■ FUNCTIONAL SPECIFICATION AND APPLICATION CIRCUIT

### 1. Reset Timing



(VDD1 1.65 - 3.5V, T<sub>A</sub> +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t <sub>R</sub>	Reset time	-	-	2.0	μs	
t <sub>RW</sub>	Reset low pulse width	10.0	-	-	μs	

(VDD1 2.4 - 3.5V, T<sub>A</sub> +25°C)

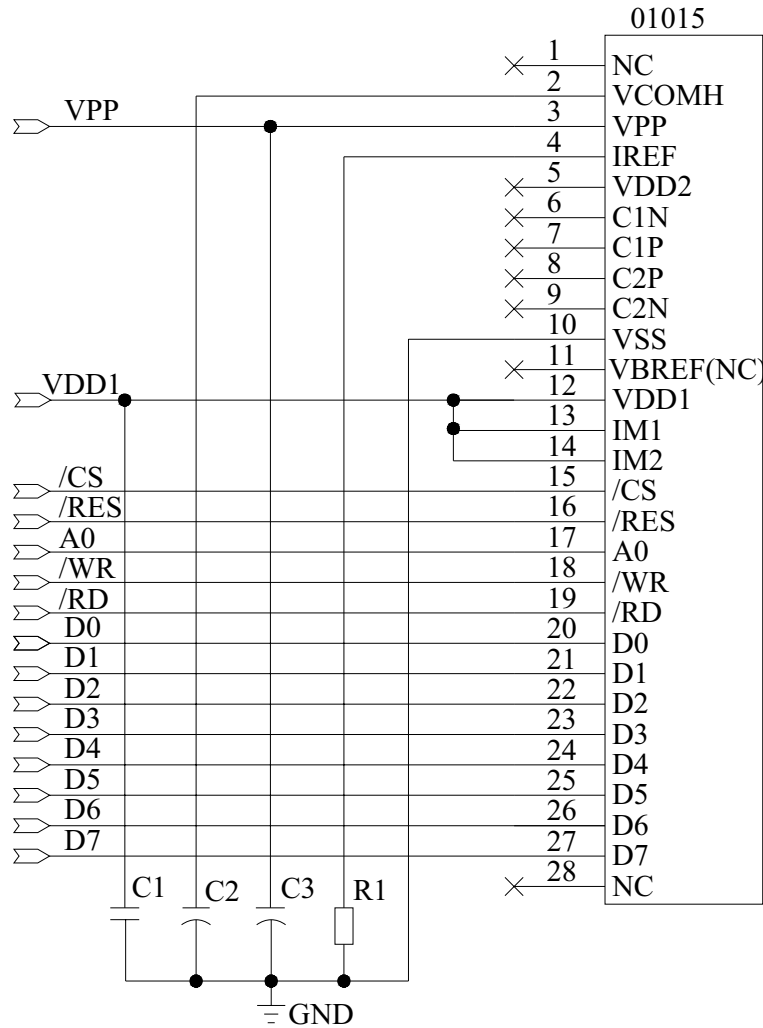
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t <sub>R</sub>	Reset time	-	-	1.0	μs	
t <sub>RW</sub>	Reset low pulse width	5.0	-	-	μs	

## 2. Application Circuit

2.1 Under external VPP Mode, the charge Pump Setting (ADh) must be set as follow:

ADh: Charge Pump Setting                      8Ah: Disable Charge Pump

(1). The configuration for 8080-parallel interface mode, external VPP is shown in the following diagram:



Pin connected to MCU interface: D[0:7], /RD, /WR, A0, /RES, /CS

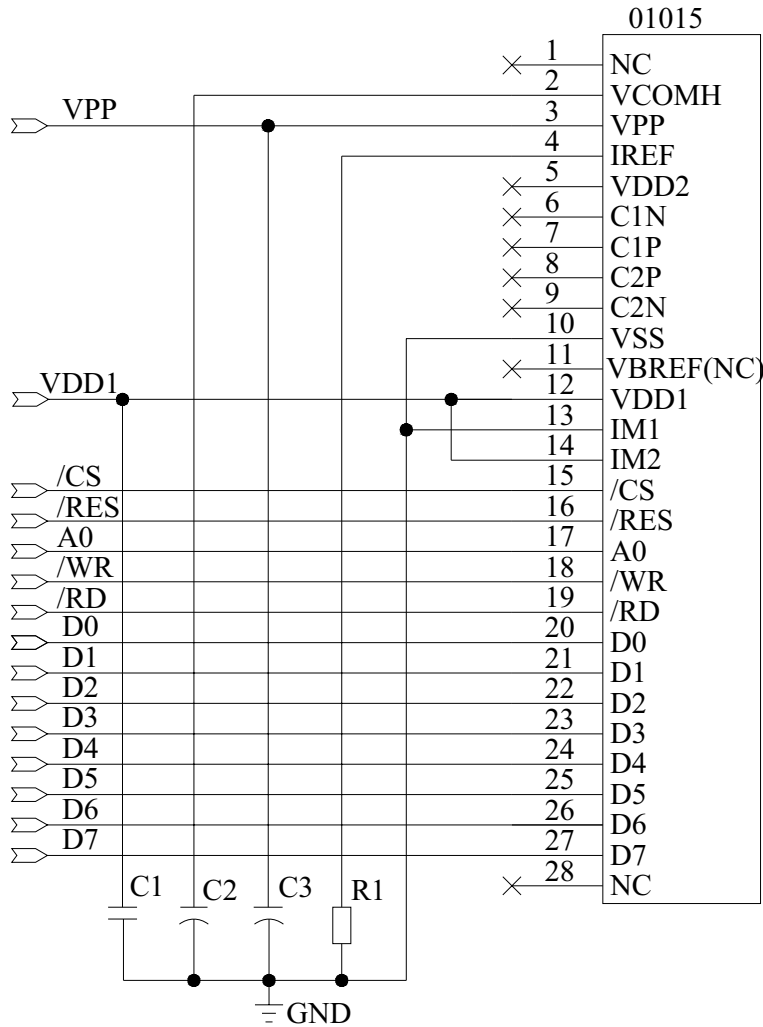
### Recommended components

C1: 1uF-0603-X7R±10%.ROHS

C2,C3 : 4.7µF/25V.ROHS (Tantalum Capacitors)

R1: 0603 1/10W +/-5% 910K ohm.ROHS

(2).The configuration for 6800-parallel interface mode, external VPP is shown in the following diagram:



Pin connected to MCU interface: D[0:7],/RD, /WR, A0,/RES , /CS

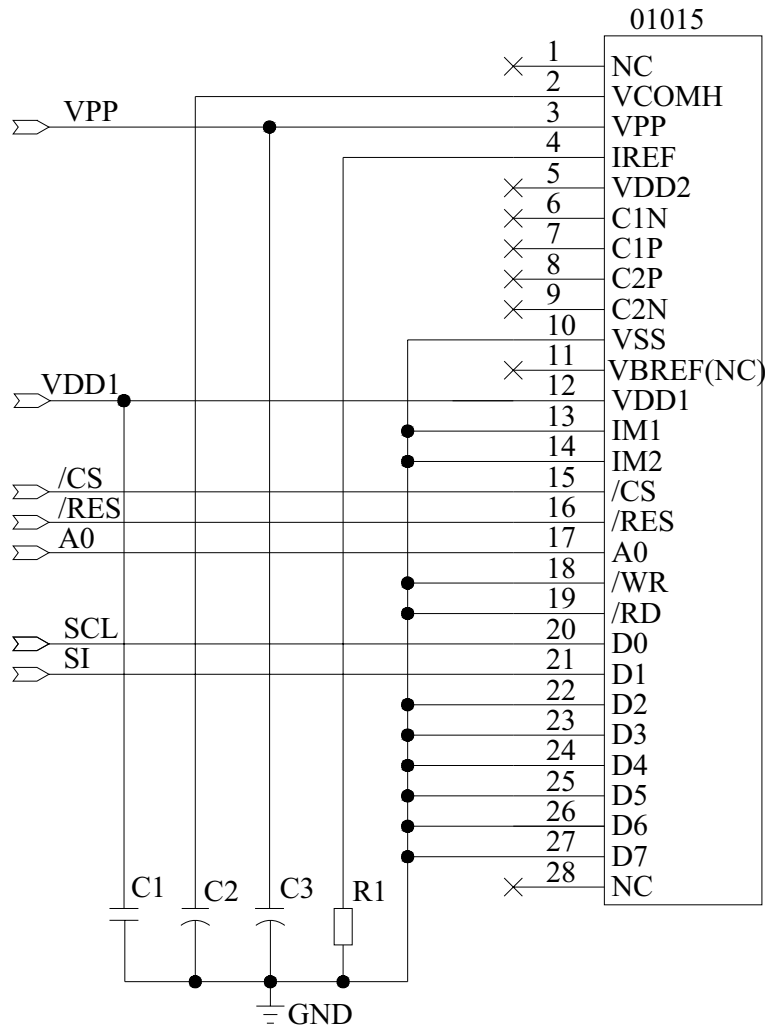
### Recommended components

C1: 1uF-0603-X7R±10%.ROHS

C2,C3 : 4.7µF/25V.ROHS (Tantalum Capacitors)

R1: 0603 1/10W +/-5% 910K ohm.ROHS

(3).The configuration for 4-wire SPI interface mode, external VPP is shown in the following diagram:



Pin connected to MCU interface: SCL,SI, /CS,A0,/RES

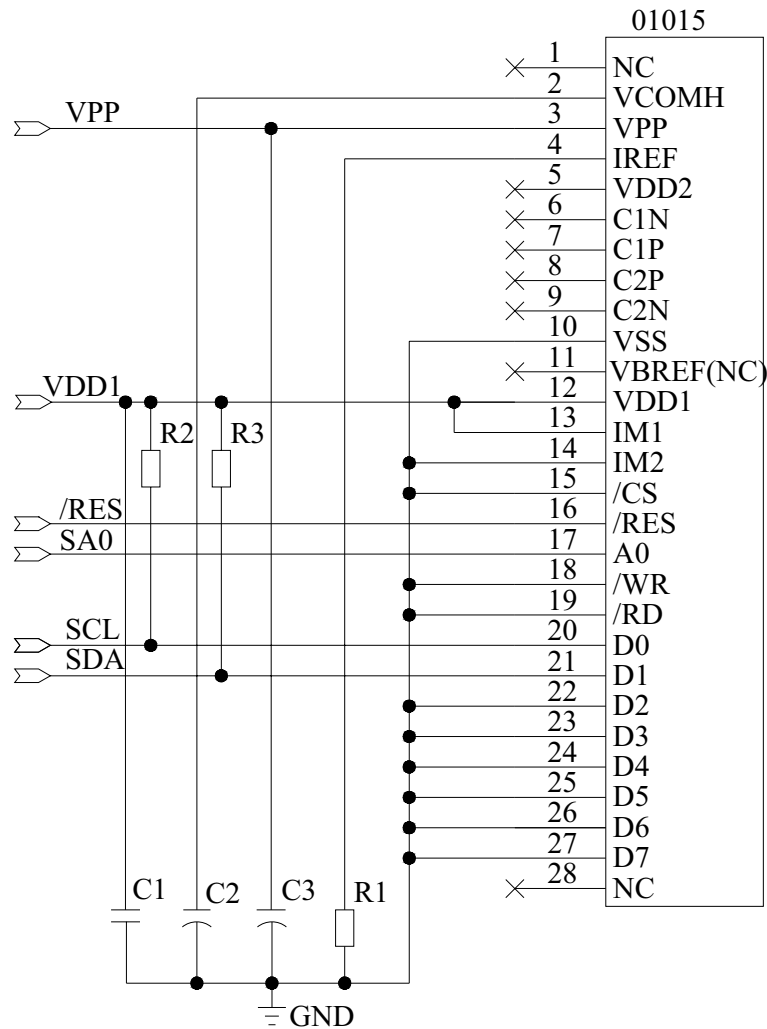
### Recommended components

C1 : 1uF-0603-X7R±10%.ROHS

C2,C3 : 4.7µF/25V.ROHS (Tantalum Capacitors)

R1: 0603 1/10W +/-5% 910K ohm.ROHS

(4).The configuration for I<sup>2</sup>C interface mode, external VPP is shown in the following diagram:



Pin connected to MCU interface: SCL,SDA, SA0,/RES

SA0	Slave address
0	0X78
1	0X7A

### Recommended components

C1: 1uF-0603-X7R±10%.ROHS

C2,C3 : 4.7µF/25V.ROHS (Tantalum Capacitors)

R1: 0603 1/10W +/-5% 910K ohm.ROHS

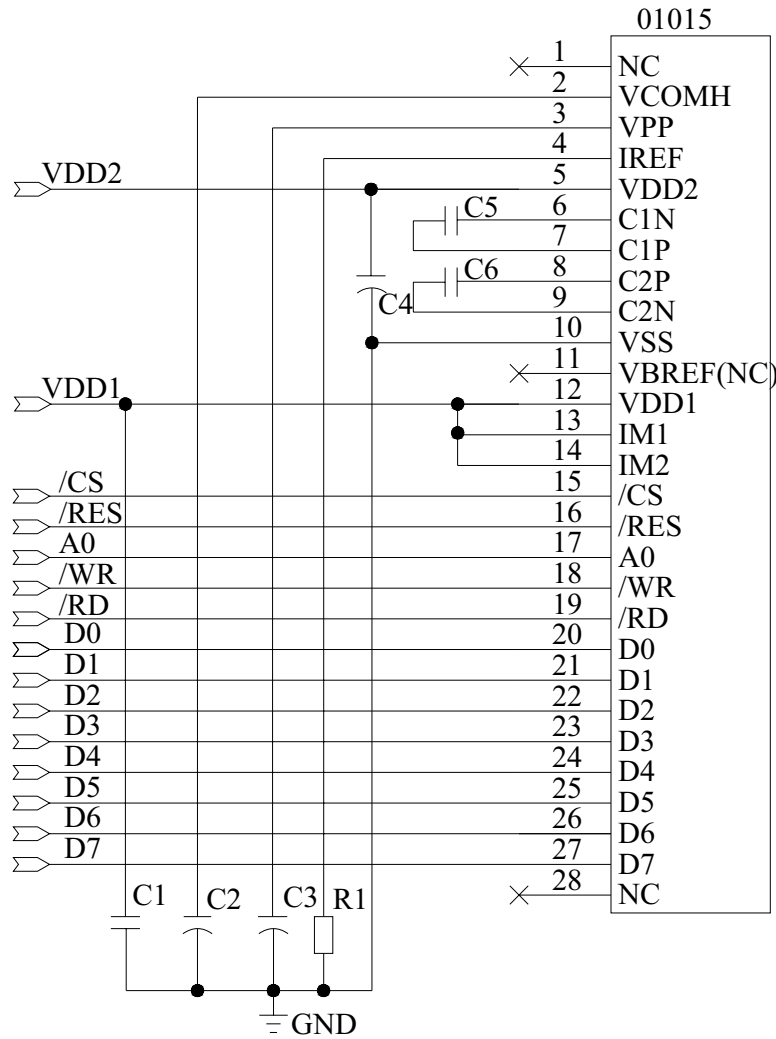
R2, R3: 0603 1/10W +/-5% 10K ohm.ROHS



2.2 Under Internal DC/DC Mode, the charge Pump Setting (ADh) must be set as follow:

ADh: Charge Pump Setting 8Bh: Enable Charge Pump

The configuration for 8080-parallel interface mode, VPP Generated by Internal DC/DC Circuit is shown in the following diagram:



Pin connected to MCU interface: D[0:7], /RD, /WR, A0, /RES, /CS

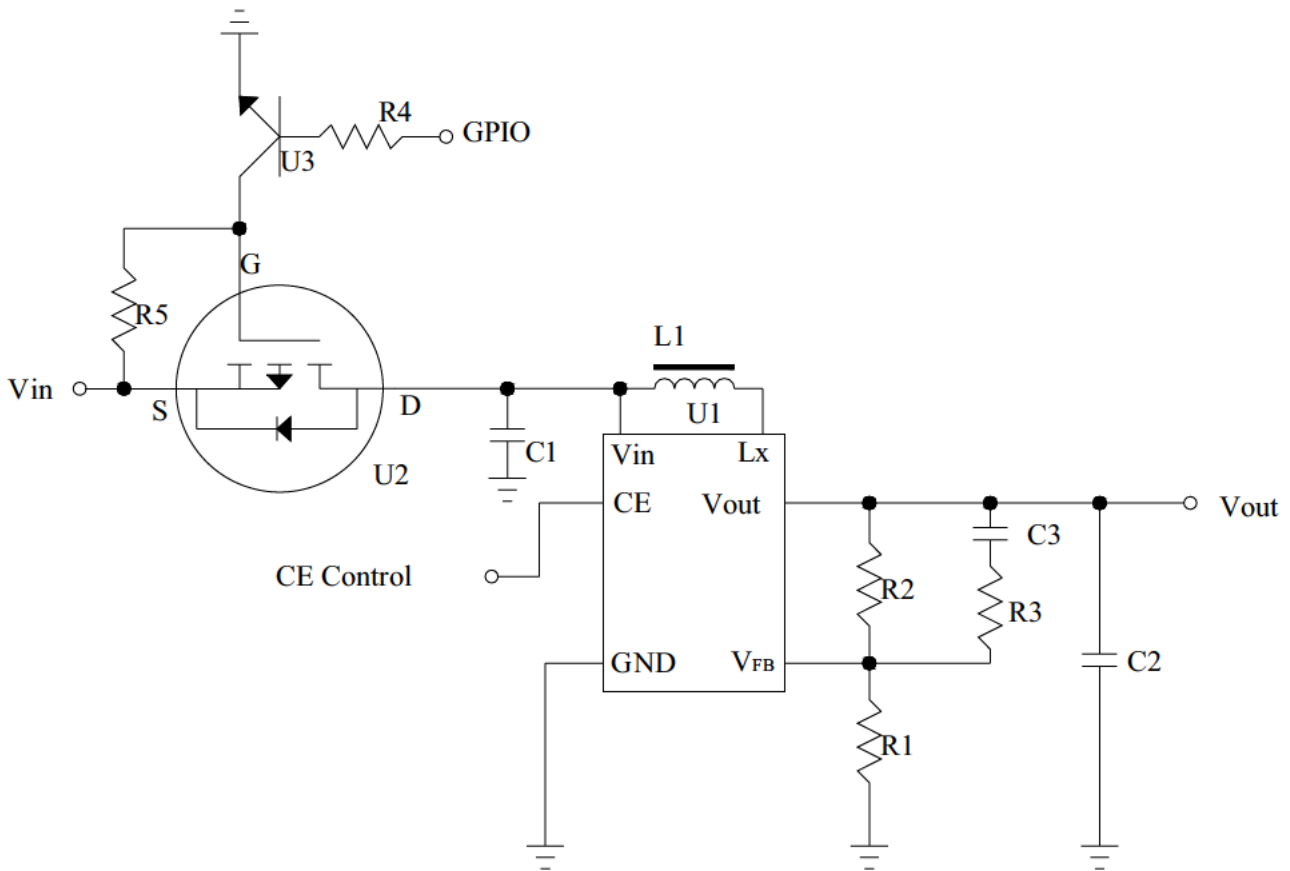
### Recommended components

C1, C5, C6: 1uF-0603-X7R±10%.ROHS

C2,C3,C4 : 4.7µF/25V.ROHS (Tantalum Capacitors)

R1: 0603 1/10W +/-5% 910K ohm.ROHS

### 3. External DC-DC application circuit



#### Recommend component

The C1	: 1 uF-0603-X7R±10%.ROHS
The C2	: 1 uF-0603-X7R±10%.ROHS
The C3	: 220pF-0603-X7R±10%.ROHS
The R1	: 0603 1/10W +/-5% 10Kohm.ROHS
The R2	: 0603 1/10W +/-5% 80Kohm.ROHS
The R3	: 0603 1/10W +/-5% 2Kohm.ROHS
The R4	: 0603 1/10W +/-5% 1Kohm.ROHS
The R5	: 0603 1/10W +/-5% 10Kohm.ROHS
The L1	: 22uH
The U1	: R1200
The U2	: FDN338P
The U3	: 8050

#### 4. Display Control Instruction

Refer to SH1106G IC Specification.

#### 5. Recommended Software Initialization

```

void Init_IC()
{
    Write_Command(0xAE); //Display Off
    Write_Command(0xD5); //Divide Ratio/Oscillator Frequency Mode Set

    Write_Command(0xC1); //
    Write_Command(0xA8); //Multiplex Ration Mode Set

    Write_Command(0x23); //
    Write_Command(0xD3); //Display Offset Mode Set

    Write_Command(0x0e); //
    Write_Command(0x40); //Set Display Start Line

    Write_Command(0xAD); //DC-DC Control Mode Set
    Write_Command(0x8b); //DC-DC ON/OFF Mode Set
    Write_Command(0x33); //Set Pump voltage value
    Write_Command(0xA1); //Set Segment Re-map
    Write_Command(0xC8); //Set Common Output Scan Direction:
    Write_Command(0xDA); //Common Pads Hardware Configuration Mode Set

    Write_Command(0x12); //
    Write_Command(0x81); //The Contrast Control Mode Set

    Write_Command(0xa3); //
    Write_Command(0xD9); //Pre-charge Period Mode Set:

    Write_Command(0x1f); //
    Write_Command(0xDB); //VCOM Deselect Level Mode Set

    Write_Command(0x40); //
    Write_Command(0xA4); //Set Entire Display OFF/ON
    Write_Command(0xA6); //Set Normal/Reverse Display

    Write_Command(0xAF); //Display On
}

```

■ **ELECTRO-OPTICAL CHARACTERISTICS (Ta=25°C)**

ITEM	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Normal Mode Brightness	L <sub>br</sub>	All pixels ON(1) (VPP generated by internal DC/DC)	300	360	-	cd/m <sup>2</sup>
Normal Mode Power Consumption	Pt	All pixels ON(1) (VPP generated by internal DC/DC)	-	138.75	166.5	mW
Sleep mode current consumption in VDD1 & VDD2(2)	ISP	During sleep, TA = +25°C, VDD1 = 3V, VDD2 = 3V. (2)	-	-	10	uA
Sleep mode current consumption in VPP		During sleep, TA = +25°C, VPP = 9V	-	-	10	uA
C.I.E(White)	(x)	x,y(CIE1931)	0.26	0.30	0.34	-
	(y)		0.29	0.33	0.37	-
Dark Room Contrast	CR	-	≥2000:1	-	-	-
Response Time	-	-	-	10	-	μ s
View Angle	-	-	≥160	-	-	Degree

Note(1): Normal Mode test conditions are as follows:

- Driving voltage : VDD2:3.7V(VPP Generated by Internal DC/DC).
- Contrast setting : 0XA3
- Frame rate : 102Hz
- Duty setting : 1/36

Note(2): Sleep Mode test conditions are as follows:

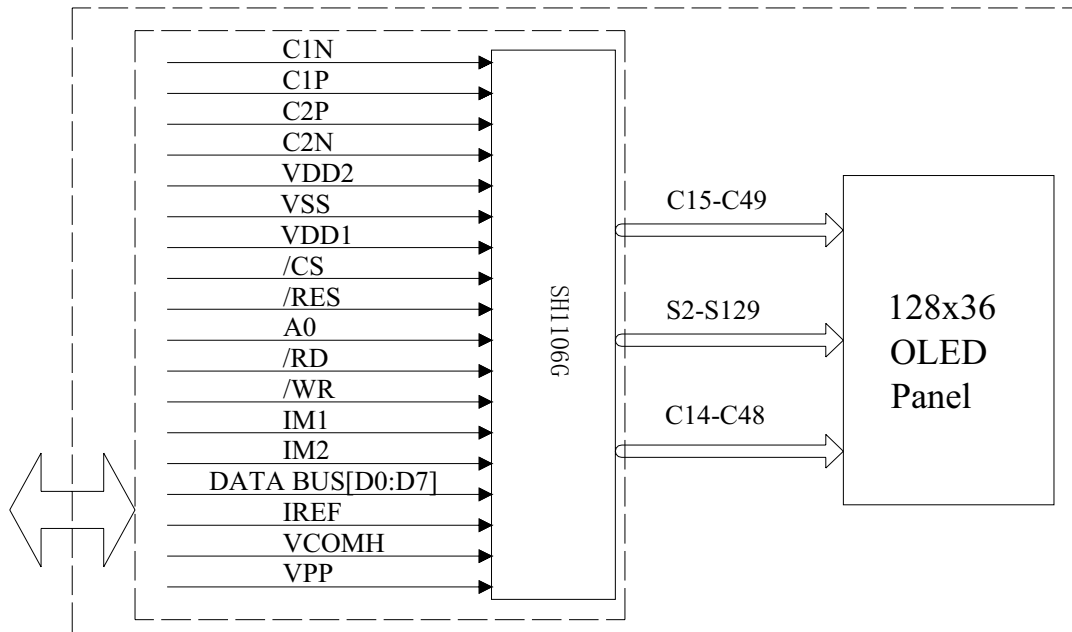
Disable Charge Pump:0XAD,0X8A.

Set Display OFF:0XAE ,

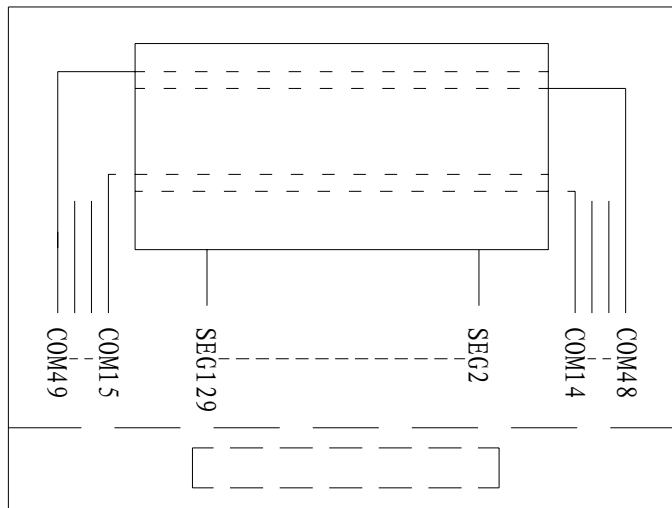
When the display OFF command is executed, power saver mode will be entered.

## ■ INTERFACE PIN CONNECTIONS

### 1 Function Block Diagram



### 2 Panel Layout Diagram



Com & Seg layout

### 3 Module Interface

PIN NO.	PIN NAME	DESCRIPTION															
1	NC	No Connection.															
2	VCOMH	This is a pad for the voltage output high level for common signals. A capacitor should be connected between this pad and VSS.															
3	VPP	OLED panel power supply. Generated by internal charge pump. Connect to capacitor. It could be supplied externally.															
4	IREF	This is a segment current reference pad. A resistor should be connected between this pad and VSS. Set the current at 10 $\mu$ A.															
5	VDD2	3.0 – 4.2V power supply pad for Power supply for charge pump circuit. This pin can be disconnected or connect to VDD1 when VPP is supplied externally.															
6	C1N	Connect to charge pump capacitor.															
7	C1P																
8	C2P																
9	C2N																
10	VSS	Ground.															
11	VBREF(NC)	This is an internal voltage reference pad for booster circuit. Keep floating.															
12	VDD1	Power supply input: 1.65 - 3.5V															
13	IM1	<table border="1"> <thead> <tr> <th>Pin Name</th> <th>I<sup>2</sup>C</th> <th>6800</th> <th>8080</th> <th>4-SPI</th> </tr> </thead> <tbody> <tr> <td>IM1</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>IM2</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	Pin Name	I <sup>2</sup> C	6800	8080	4-SPI	IM1	1	0	1	0	IM2	0	1	1	0
Pin Name	I <sup>2</sup> C	6800	8080	4-SPI													
IM1	1	0	1	0													
IM2	0	1	1	0													
14	IM2																
15	/CS	This pad is the chip select input. When /CS = “L”, then the chip select becomes active, and data/command I/O is enabled.															
16	/RES	This is a reset signal input pad. When /RES is set to “L”, the settings are initialized. The reset operation is performed by the /RES signal level.															
17	A0	This is the Data/Command control pad that determines whether the data bits are data or a command. A0 = “H”: the inputs at D0 to D7 are treated as display data. A0 = “L”: the inputs at D0 to D7 are transferred to the command registers. In I <sup>2</sup> C interface, this pad serves as SA0 to distinguish the different address of OLED driver.															
18	/WR	This is a MPU interface input pad. When connected to an 8080 MPU, this is active LOW. This pad connects to the 8080 MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal. When connected to a 6800 Series MPU: This is the read/write control signal input terminal. When /WR = “H”: Read. When /WR = “L”: Write.															
19	/RD	This is a MPU interface input pad. When connected to an 8080 series MPU, it is active LOW. This pad is connected to the /RD signal of the 8080 series MPU, and the data bus is in an output status when this signal is “L”. When connected to a 6800 series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU. When /RD = “H”: Enable. When /RD = “L”: Disable.															
20~27	D0~D7	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SI). At this time, D2 to D7 are set to high impedance. When the I <sup>2</sup> C interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SDAI). At this time, D2 to D7 are set to high impedance.															
28	NC	No Connection.															

■ **RELIABILITY TESTS**

Item		Condition	Criterion
High Temperature Storage (HTS)		85±2°C, 240 hours	<ol style="list-style-type: none"> <li>1. After testing, the function test is ok.</li> <li>2. After testing, no addition to the defect.</li> <li>3. After testing, the change of luminance should be within +/- 50% of initial value.</li> <li>4. After testing, the change for the mono and area color must be within (+/-0.02, +/- 0.02) and for the full color it must be within (+/-0.04, +/-0.04) of initial value based on 1931 CIE coordinates.</li> <li>5. After testing, the change of total current consumption should be within +/- 50% of initial value.</li> </ol>
High Temperature Operating (HTO)		70±2°C, 240 hours	
Low Temperature Storage (LTS)		-40±2°C, 240 hours	
Low Temperature Operating (LTO)		-40±2°C, 240 hours	
High Temperature / High Humidity Storage (HTHHS)		60±3°C, 90%±3%RH, 240 hours	
Thermal Shock (Non-operation) (TS)		-40±2°C ~ 25°C ~ 85±2°C (30min) (5min) (30min) 30cycles	
Vibration (Packing)	10~55~10Hz, amplitude 1.5mm, 1 hour for each direction x, y, z	<ol style="list-style-type: none"> <li>1. One box for each test.</li> <li>2. No addition to the cosmetic and the electrical defects.</li> </ol>	
Drop (Packing)	Height : 1 m, each time for 6 sides, 3 edges, 1 angle		

Note: 1) For each reliability test, the sample quantity is 3, and only for one test item.  
 2) The HTHHS test is requested the Pure Water(Resistance > 10MΩ).

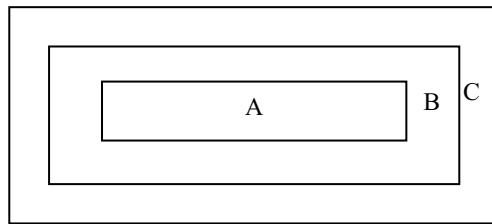
## ■ OUTGOING QUALITY CONTROL SPECIFICATION

### ◆ Standard

According to GB/T2828.1-2003/ISO 2859-1: 1999 and ANSI/ASQC Z1.4-1993, General Inspection Level II.

### ◆ Definition

- 1 Major defect : The defect that greatly affect the usability of product.
- 2 Minor defect : The other defects, such as cosmetic defects, etc.
- 3 Definition of inspection zone:



Zone A: Active Area

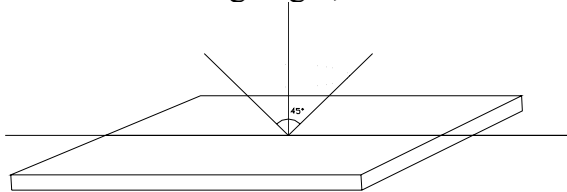
Zone B: Viewing Area except Zone A

Zone C: Outside Viewing Area

Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble of quality and assembly to customer's product.

### ◆ Inspection Methods

- 1 The general inspection : under 20W x 2 or 40W fluorescent light, about 30cm viewing distance, within 45° viewing angle, under 25±5°C.



- 2 The luminance and color coordinate inspection : By PR705 or BM-7 or the equal equipments, in the dark room, under 25±5°C.

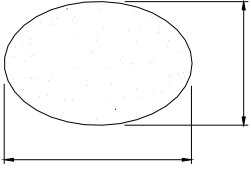
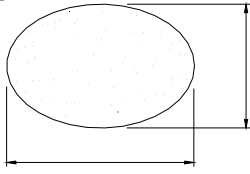
### ◆ Inspection Criteria

- 1 Major defect : AQL= 0.65

Item	Criterion
Function Defect	1. No display or abnormal display is not accepted
	2. Open or short is not accepted.
	3. Power consumption exceeding the spec is not accepted.
Outline Dimension	Outline dimension exceeding the spec is not accepted.
Glass Crack	Glass crack tends to enlarge is not accepted.

- 2 Minor Defect : AQL= 1.5



Item	Criterion				
Spot Defect (dimming and lighting spot)	Size (mm)		Accepted Qty		
			Area A + Area B	Area C	
		$\Phi \leq 0.10$		Ignored	
		$0.10 < \Phi \leq 0.15$		3	Ignored
		$0.15 < \Phi \leq 0.20$		1	
$0.20 < \Phi$		0			
Note : $\Phi = (x + y) / 2$					
Line Defect (dimming and lighting line)	L ( Length ) : mm	W ( Width ) : mm	Area A + Area B	Area C	
	/	$W \leq 0.03$	Ignored		
	$L \leq 3.0$	$0.03 < W \leq 0.05$	2	Ignored	
	$L \leq 2.0$	$0.05 < W \leq 0.08$	1		
	/	$0.08 < W$	As spot defect		
Remarks: The total of spot defect and line defect shall not exceed 4 pcs.					
Polarizer Stain	Stain which can be wiped off lightly with a soft cloth or similar cleaning is accepted, otherwise, according to the Spot Defect and the Line Defect.				
Polarizer Scratch	1. If scratch can be seen during operation, according to the criterions of the Spot Defect and the Line Defect.				
	2. If scratch can be seen only under non-operation or some special angle, the criterion is as below :				
	L ( Length ) : mm	W ( Width ) : mm	Area A + Area B	Area C	
	/	$W \leq 0.03$	Ignore		
	$5.0 < L \leq 10.0$	$0.03 < W \leq 0.05$	2	Ignore	
	$L \leq 5.0$	$0.05 < W \leq 0.08$	1		
/	$0.08 < W$	0			
Polarizer Air Bubble	Size		Area A + Area B	Area C	
		$\Phi \leq 0.20$		Ignored	
		$0.20 < \Phi \leq 0.50$		2	Ignored
		$0.50 < \Phi \leq 0.80$		1	
		$0.80 < \Phi$		0	

Glass Defect (Glass Chipped )	1. On the corner	(mm)	<table border="1"> <tr> <td>x</td> <td><math>\leq 2.0</math></td> </tr> <tr> <td>y</td> <td><math>\leq S</math></td> </tr> <tr> <td>z</td> <td><math>\leq t</math></td> </tr> </table>	x	$\leq 2.0$	y	$\leq S$	z	$\leq t$
	x	$\leq 2.0$							
	y	$\leq S$							
	z	$\leq t$							
2. On the bonding edge	(mm)	<table border="1"> <tr> <td>x</td> <td><math>\leq a / 2</math></td> </tr> <tr> <td>y</td> <td><math>\leq s / 3</math></td> </tr> <tr> <td>z</td> <td><math>\leq t</math></td> </tr> </table>	x	$\leq a / 2$	y	$\leq s / 3$	z	$\leq t$	
x	$\leq a / 2$								
y	$\leq s / 3$								
z	$\leq t$								
3. On the other edges	(mm)	<table border="1"> <tr> <td>x</td> <td><math>\leq a / 5</math></td> </tr> <tr> <td>y</td> <td><math>\leq 1.0</math></td> </tr> <tr> <td>z</td> <td><math>\leq t</math></td> </tr> </table>	x	$\leq a / 5$	y	$\leq 1.0$	z	$\leq t$	
x	$\leq a / 5$								
y	$\leq 1.0$								
z	$\leq t$								
Note: t: glass thickness ; s: pad width ; a: the length of the edge									
TCP Defect	Crack, deep fold and deep pressure mark on the TCP are not accepted								
Pixel Size	The tolerance of display pixel dimension should be within $\pm 20\%$ of the spec								
Luminance	Refer to the spec or the reference sample								
Color	Refer to the spec or the reference sample								

## ■ CAUTIONS IN USING OLED MODULE

### ◆ Precautions For Handling OLED Module:

1. OLED module consists of glass and polarizer. Pay attention to the following items when handling:
  - i. Avoid drop from high, avoid excessive impact and pressure.
  - ii. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead.
  - iii. If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
  - iv. Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
  - v. Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
  - vi. Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of iii.
2. Do not attempt to disassemble or process the OLED Module.
3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.
4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.
5. Be sure to keep the air pressure under 120 kPa, otherwise the glass cover is to be cracked.
6. Be careful to prevent damage by static electricity:
  - i. Be sure to ground the body when handling the OLED Modules.
  - ii. All machines and tools required for assembling, such as soldering irons, must be properly grounded.
  - iii. Do not assemble and do no other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%-60% is recommended.
  - iv. Peel off the protective film slowly to avoid the amount of static electricity generated.
  - v. Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.
  - vi. Be sure to use anti-static package.
7. Contamination on terminals can cause an electrochemical reaction and corrode the terminal circuit, so make it clean anytime.
8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.
9. When the logic circuit power is off, do not apply the input signals.
10. Power on sequence:  $V_{DD} \rightarrow V_{PP}$ , and power off sequence:  $V_{PP} \rightarrow V_{DD}$ .
11. Be sure to keep temperature, humidity and voltage within the ranges of the spec, otherwise shorten Module's life time, even make it damaged.
12. Be sure to drive the OLED Module following the Specification and Datasheet of IC controller, otherwise something wrong may be seen.



13. When displaying images, keep them rolling, and avoid one fixed image displaying more than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

## ◆ **Precautions For Soldering OLED Module:**

1. Soldering temperature :  $260^{\circ}\text{C} \pm 10^{\circ}\text{C}$ .
2. Soldering time : 3-4 sec.
3. Repeating time : no more than 3 times.
4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

## ◆ **Precautions For Storing OLED Module:**

1. Be sure to store the OLED Module in the vacuum bag with dessicant.
2. If the Module can not be used up in 1 month after the bag being opened, make sure to seal the Module in the vacuum bag with dessicant again.
3. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
4. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
5. It is recommended to keep the temperature between  $0^{\circ}\text{C}$  and  $30^{\circ}\text{C}$  , the relative humidity not over 60%.

## ◆ **Limited Warranty**

Unless relevant quality agreements signed with customer and law enforcement, for a period of 12 months from date of production, all products (except automotive products) All Shore will replace or repair any of its OLED modules which are found to be functional defect when inspected in accordance with All Shore standards (copies available upon request). Cosmetic/visual defects must be returned to All Shore within 90 days of shipment. Confirmation of such date should be based on freight documents. The warranty liability of All Shore is limited to repair and/or replacement on the terms above. All Shore will not be responsible for any subsequent or consequential events.

## ◆ **Return OLED Module Under Warranty:**

1. No warranty in the case that the precautions are disregarded.
2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects.